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A	<div><div>THIS DRAWING AND SPECIFICATIONS, HEREIN, ARE THE PROPERTY OF INVENTEC CORPORATION AND SHALL NOT BE REPRODUCED, COPIED, OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION. INVENTEC CORPORATION 2009 ALL RIGHT RESERVED</div><div><div>Sarah AMD-Sabine 15"</div><div>DB</div><div>www.altech1.ru</div><div>2010/08/24</div></div></div>																																																																																								
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DATE	CHANGE NO.	REV																																																																																							
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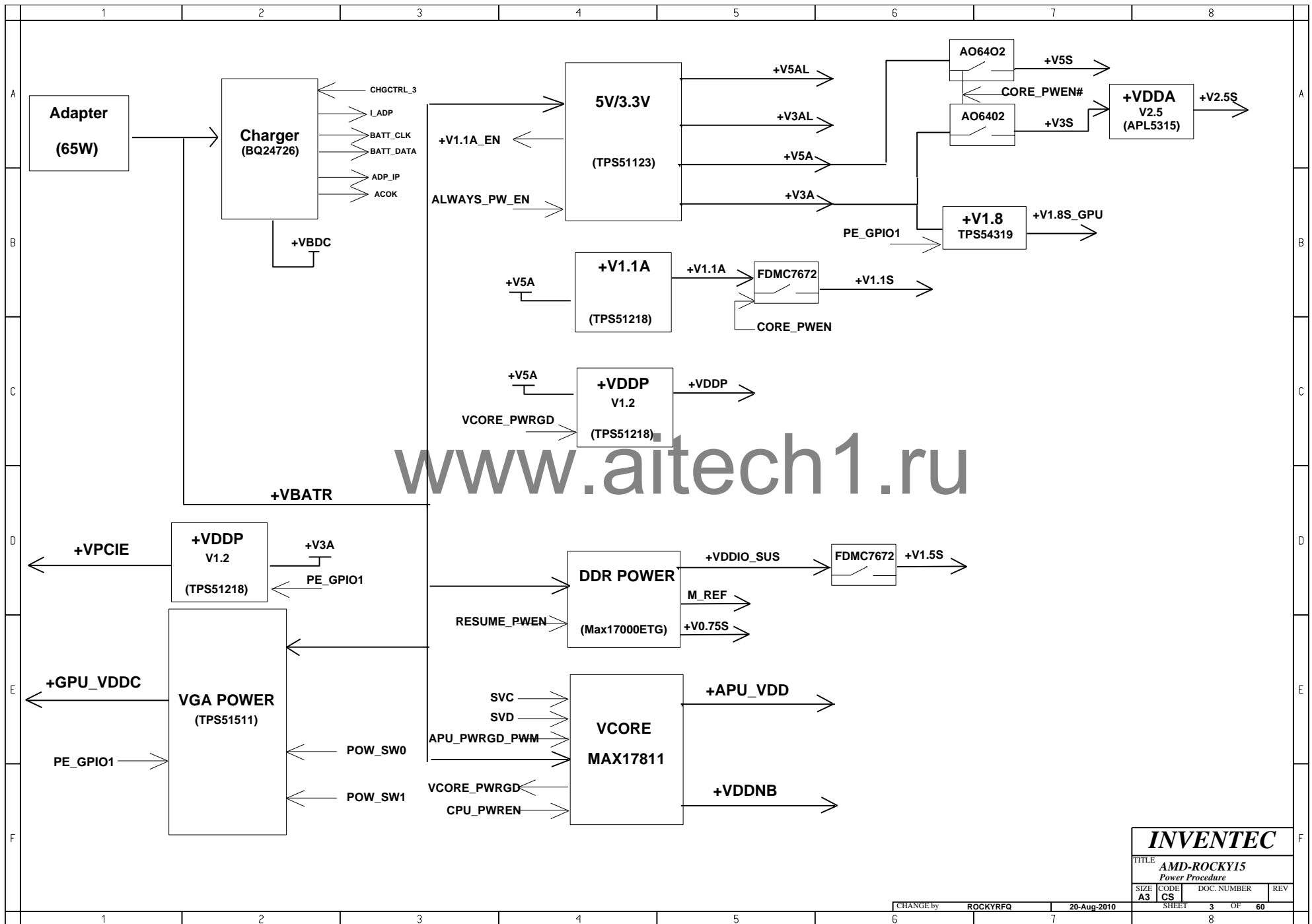
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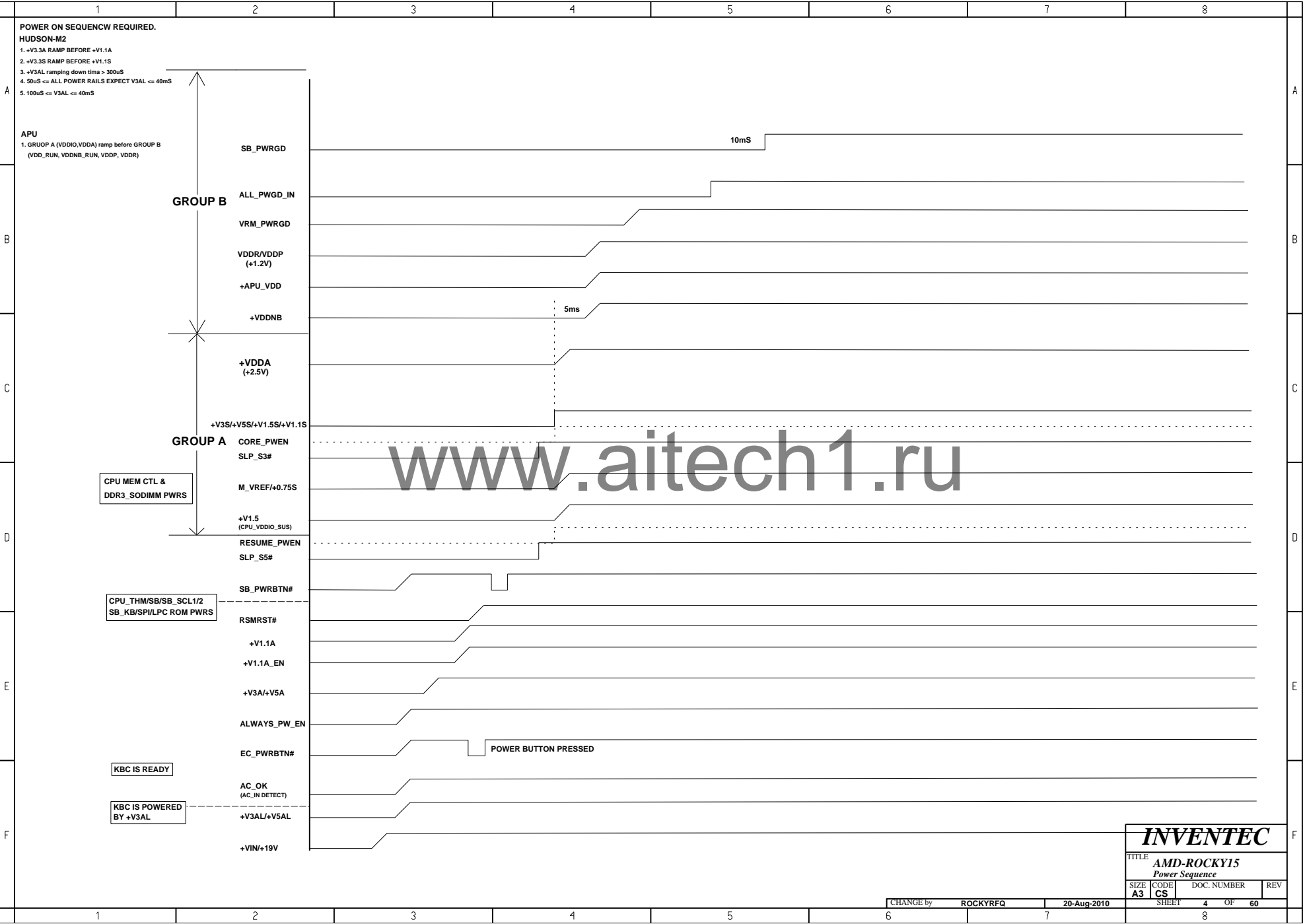
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TITLE: **AMD-ROCKY15**
Power Procedure

SIZE: **A3** CODE: **CS** DOC. NUMBER: **3** OF **60** REV: **8**

CHANGE by: **ROCKYRFQ** 20-Aug-2010

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TITLE
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Power Sequence

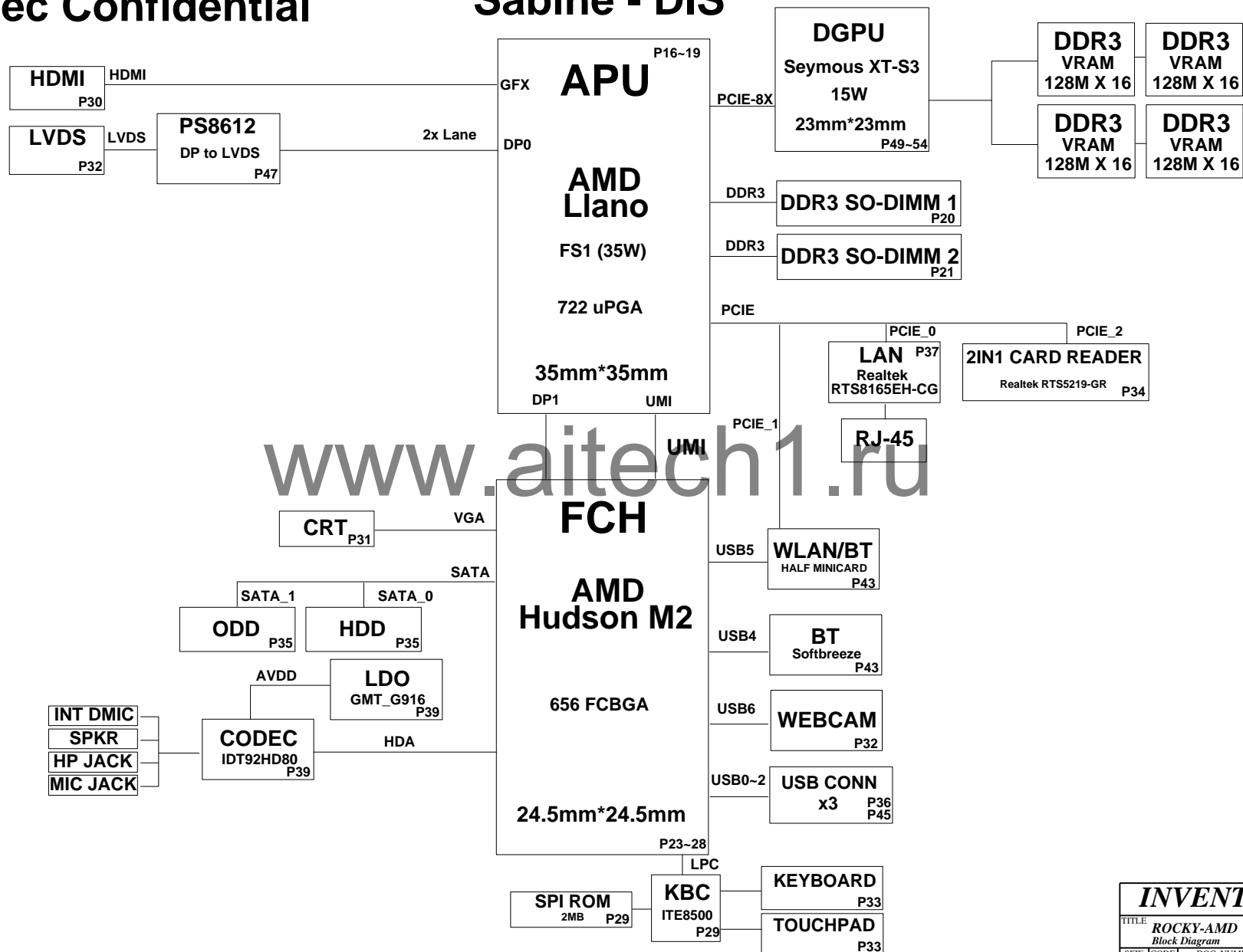
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CHANGE by ROCKYRFQ 20-Aug-2010

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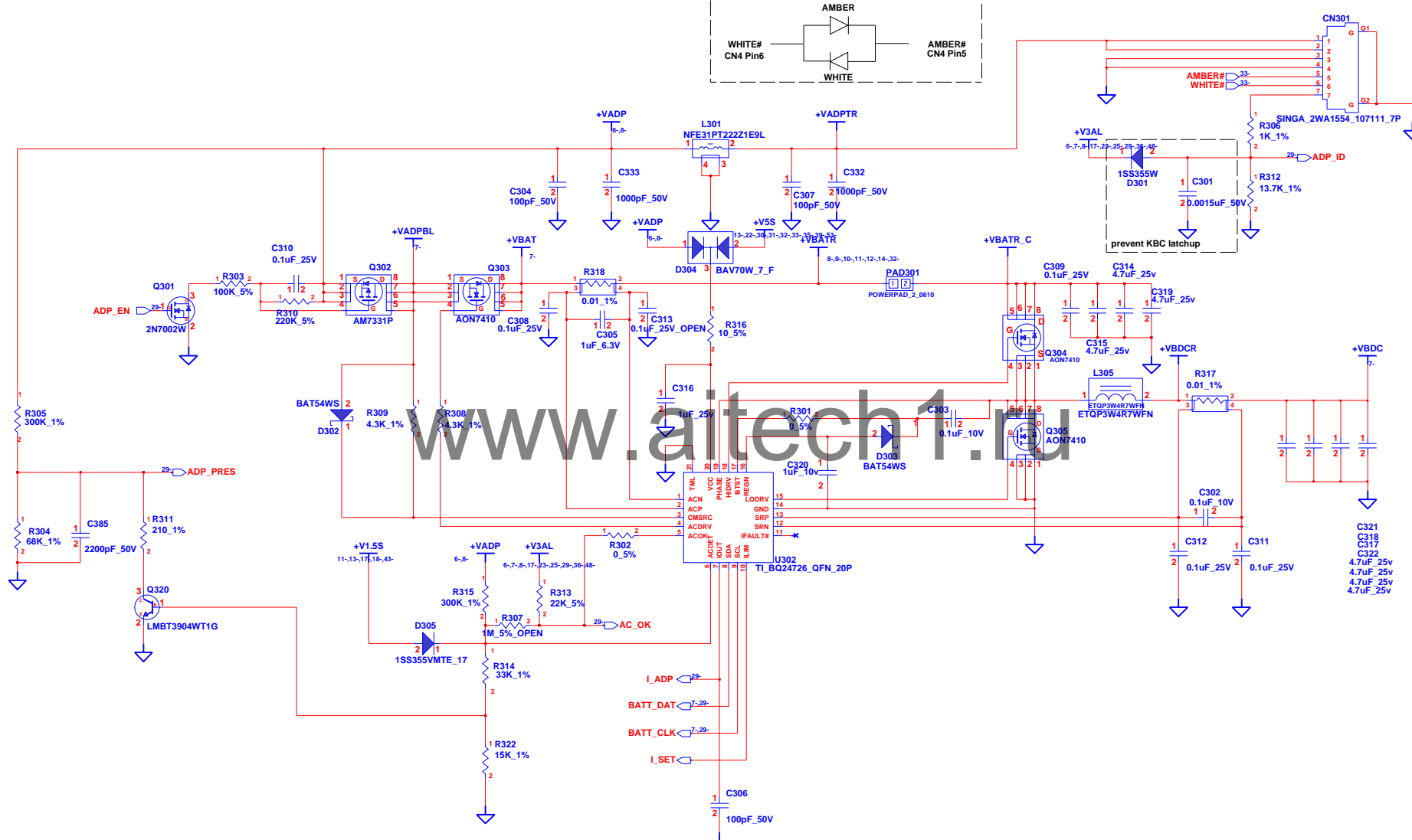
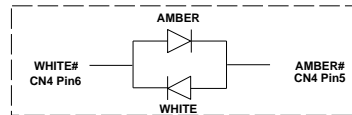
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CHANGE by	<i>Ken, Chiang</i>	20-Aug-2010
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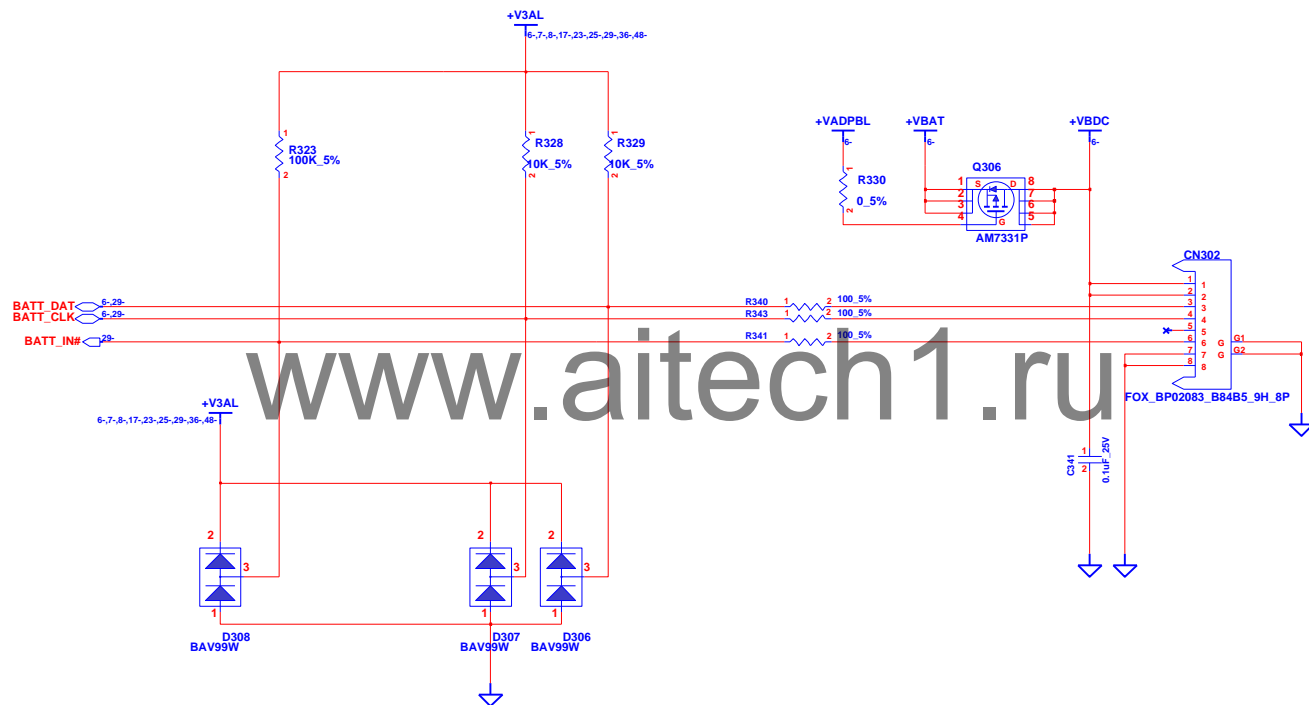


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TITLE ROCKY-AMD DC & BATTERY CHARGER			
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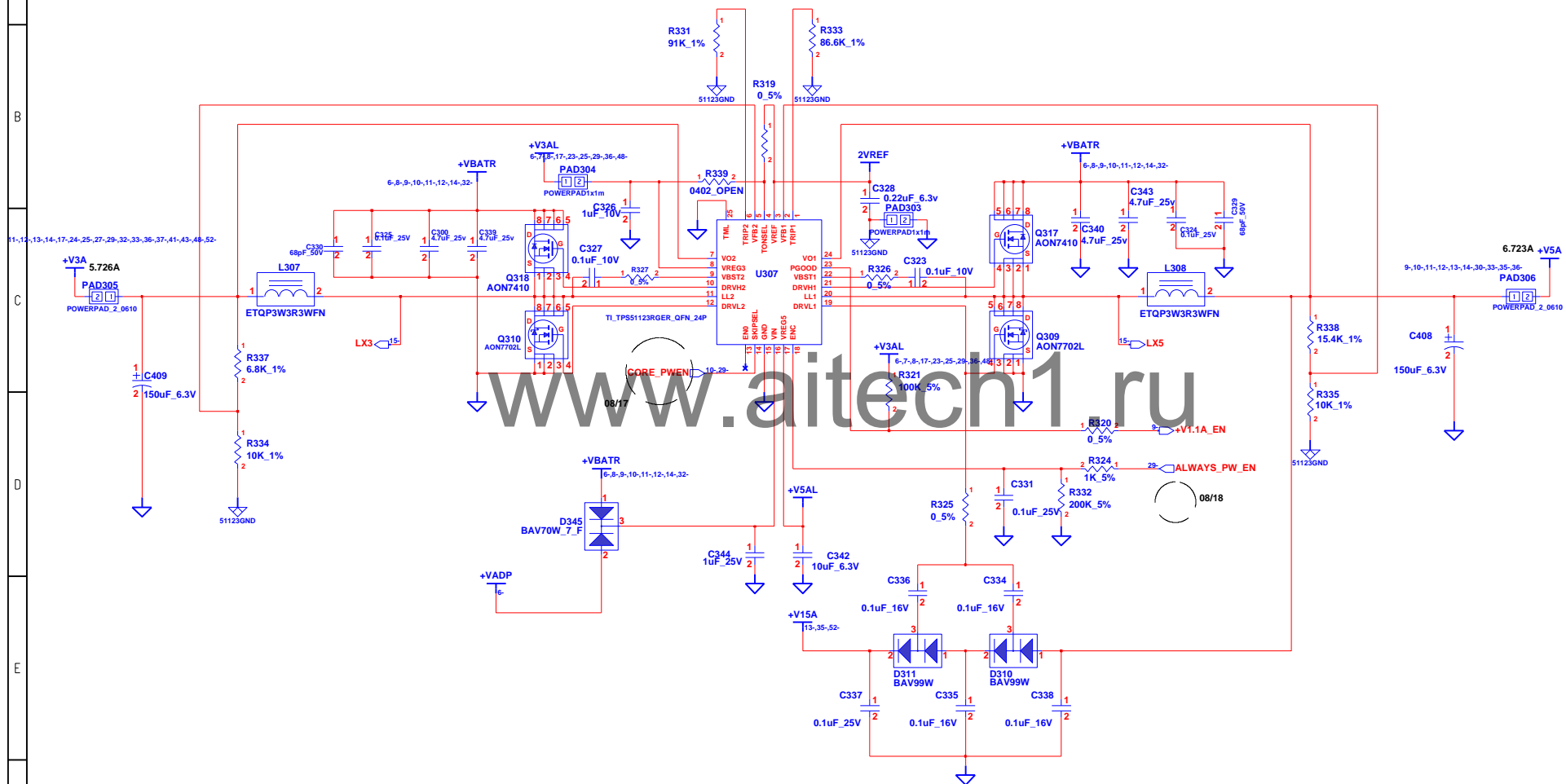
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**ROCKY-AMD
BATTERY CONN**

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CHANGE by **Ken, Chiang** 9-Aug-2010

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+V3A & +V5A



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TITLE: **ROCKY-AMD**
+V3A & +V5A

SIZE: **A3** CODE: **CS** DOC. NUMBER: **1234** REV: **X01**

CHANGE by: **Ken Chiang** 9-Aug-2010

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A



2



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+VCC_CORE & VDDIO_SUS & +V0.75S

The schematic diagram illustrates the power supply section for the ROCKY-AMD chip, specifically the +VCC_CORE, VDDIO_SUS, and +V0.75S rails. The diagram shows the following components and connections:

- Power Sources:** +V5A, +VBATR, and +V0.75S.
- Regulators:** U305 (DDR3 REGULATOR), Q314 (1A MOSFET), Q311 (FDSM0310AS), and L306 (ETQP3W1R0WTFN).
- Capacitors:** C388 (2.2uF 6.3V), C396 (0.1uF 10V), C397 (0.1uF 10V), C389 (0.01uF 50V), C393 (0.1uF 10V), C394 (0.1uF 10V), C373 (4.7uF 25V), C381 (4.7uF 25V), C391 (6.3uF 25V), C390 (68pF 50V), C372 (330uF 2V 15mR_Pana_-35%), C380 (10uF 6.3V), and C392 (0.22uF 10V).
- Resistors:** R395 (0.5%), R396 (0.5%), R390 (52.3K 1%), R393 (10K 1%), R392 (100K 5%), R391 (38.3K 1%), R763 (0.5%), and R394 (0.5%).
- Other Components:** PAD308 (POWERPAD 2.0610), PAD309 (POWERPAD1x1m), and TP551216_GND.
- Connections:** The diagram shows the connections between the power sources, regulators, capacitors, and resistors, including the +VCC_CORE, VDDIO_SUS, and +V0.75S rails.

NOTE: DDR3 REGULATOR

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ROCKY-AMD

+VCC_CORE & +VDDIO_SUS & +V0.75S

SIZE	CODE	DOC. NUMBER	REV
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CHANGE by: Ken, Chiang 9-Jun-2010

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+VCC_CORE & VDDIO_SUS & +V0.75S

The schematic diagram illustrates the power supply section for the ROCKY-AMD chip, specifically the +VCC_CORE, VDDIO_SUS, and +V0.75S rails. The diagram shows the following components and connections:

- Power Sources:** +V5A, +VBATR, and +V0.75S.
- Regulators:** U305 (DDR3 REGULATOR), Q314 (1A MOSFET), Q311 (FDSM0310AS), and L306 (ETQP3W1R0WTFN).
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- Resistors:** R395 (0.5%), R396 (0.5%), R390 (52.3K 1%), R393 (10K 1%), R392 (100K 5%), R391 (38.3K 1%), R763 (0.5%), R394 (0.5%).
- Other Components:** PAD308 (POWERPAD_2_0610), PAD309 (POWERPAD1x1m), TP551216_GND, TP551216_GND, TP551216_GND, LXMEN.
- Connections:** The diagram shows the connection of the power rails to the chip pins (VSN, VBST, DRVH, SW, SS, DRVL, POND, PGOD, VDDQSN, VLDON, VTT, VTTSN, GND, MODE, TRIP, VTTGND, VTTREF, TML) and the output of the regulators to the chip pins (VCC, VDDIO_SUS, V0.75S).

NOTE: DDR3 REGULATOR

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ROCKY-AMD

+VCC_CORE & +VDDIO_SUS & +V0.75S

SIZE	CODE	DOC. NUMBER	REV
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CHANGE by Ken, Chiang 9-Jun-2010

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+VCC_CORE & VDDIO_SUS & +V0.75S

The schematic diagram illustrates the power supply section for the ROCKY-AMD chip, specifically the +VCC_CORE, VDDIO_SUS, and +V0.75S rails. The diagram shows the following components and connections:

- Power Sources:** +V5A, +VBATR, and +V0.75S.
- Regulators:** U305 (DDR3 REGULATOR), Q314 (1A MOSFET), Q311 (FDSM0310AS), and L306 (ETQP3W1R0WTFN).
- Capacitors:** C388 (2.2uF 6.3V), C396 (0.1uF 10V), C397 (0.1uF 10V), C389 (0.01uF 50V), C393 (0.1uF 10V), C394 (0.1uF 10V), C373 (4.7uF 25V), C381 (4.7uF 25V), C391 (6.3uF 25V), C390 (68pF 50V), C372 (330uF 2V 15mR_Pana_-35%), C380 (10uF 6.3V), and C392 (0.22uF 10V).
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- Connections:** The diagram shows the connections between the power sources, regulators, capacitors, and resistors, including the +VCC_CORE, VDDIO_SUS, and +V0.75S rails.

NOTE: DDR3 REGULATOR

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ROCKY-AMD

+VCC_CORE & +VDDIO_SUS & +V0.75S

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01

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+VCC_CORE & VDDIO_SUS & +V0.75S

The schematic diagram illustrates the power supply section for the ROCKY-AMD chip, specifically the +VCC_CORE, VDDIO_SUS, and +V0.75S rails. The diagram shows the following components and connections:

- Power Input:** +V5A (5V) and +VBATR (Battery) are the main power sources.
- Regulators:**
 - U305 (TPS51216RUKR QFN 20P):** A DDR3 regulator that converts +V5A to +V0.75S. It includes pins for VSN, VBST, DRVH, SW, SS, VREF, DRVL, POND, PGOD, VDDQSN, VLDON, VTT, VTTSN, GND, MODE, TRIP, VTTGND, VTTREF, and TML.
 - Q314 (AON7410):** A 1A MOSFET used for the +VDDIO_SUS rail.
 - Q311 (FDS0310AS):** A MOSFET used for the +V0.75S rail.
- Capacitors:**
 - C388 (2.2uF 6.3V):** Input capacitor for +V5A.
 - C373 (4.7uF 25V):** Input capacitor for +VBATR.
 - C391 (6.3uF 25V):** Input capacitor for +VDDIO_SUS.
 - C390 (68pF 50V):** Output capacitor for +VDDIO_SUS.
 - C392 (0.22uF 10V):** Output capacitor for +V0.75S.
 - C380 (10uF 6.3V):** Output capacitor for +V0.75S.
 - C393 (0.1uF 10V):** Output capacitor for +V0.75S.
 - C389 (0.01uF 50V):** Output capacitor for +V0.75S.
 - C396 (0.1uF 10V_OPEN):** Output capacitor for +V0.75S.
 - C397 (0.1uF 10V_OPEN):** Output capacitor for +V0.75S.
 - C398 (0.1uF 10V_OPEN):** Output capacitor for +V0.75S.
 - C399 (0.1uF 10V_OPEN):** Output capacitor for +V0.75S.
- Resistors:**
 - R395 (0.5%):** Input resistor for +V5A.
 - R396 (0.5%):** Input resistor for +V5A.
 - R393 (10K 1%):** Input resistor for +V5A.
 - R392 (100K 5%):** Input resistor for +V5A.
 - R391 (38.3K 1%):** Input resistor for +V5A.
 - R394 (0.5%):** Input resistor for +V5A.
 - R397 (52.3K 1%):** Input resistor for +V5A.
 - R398 (52.3K 1%):** Input resistor for +V5A.
 - R399 (52.3K 1%):** Input resistor for +V5A.
- Other Components:**
 - L306 (ETQP3W1R0WTFN):** Inductor for the +VDDIO_SUS rail.
 - LXMEN:** Inductor for the +V0.75S rail.
 - PAD308 (POWERPAD_2_0610):** Power pad for the +VDDIO_SUS rail.
 - PAD309 (POWERPAD1x1m):** Power pad for the +V0.75S rail.

NOTE: DDR3 REGULATOR

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ROCKY-AMD

+VCC_CORE & +VDDIO_SUS & +V0.75S

SIZE A3 CS 1234

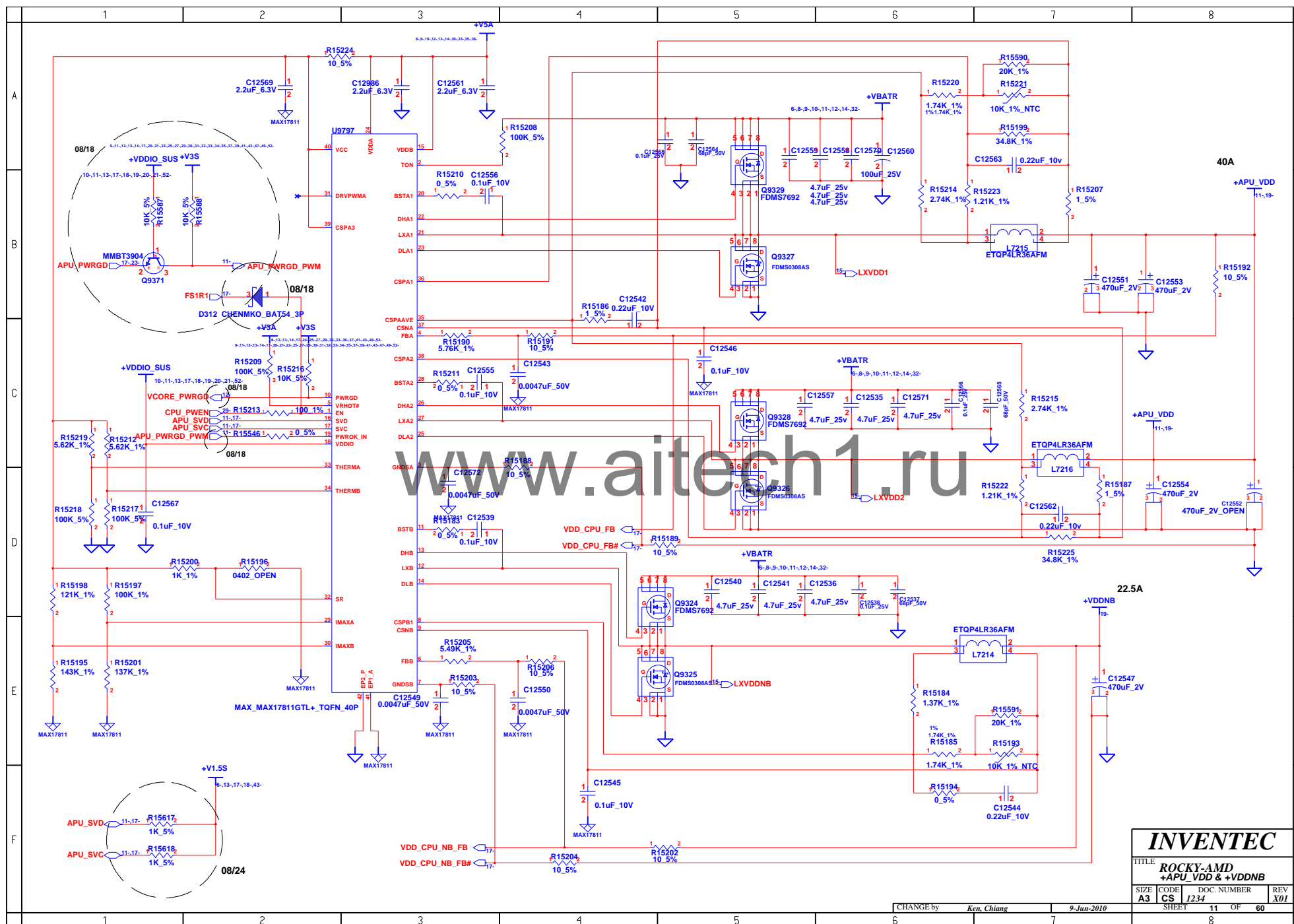
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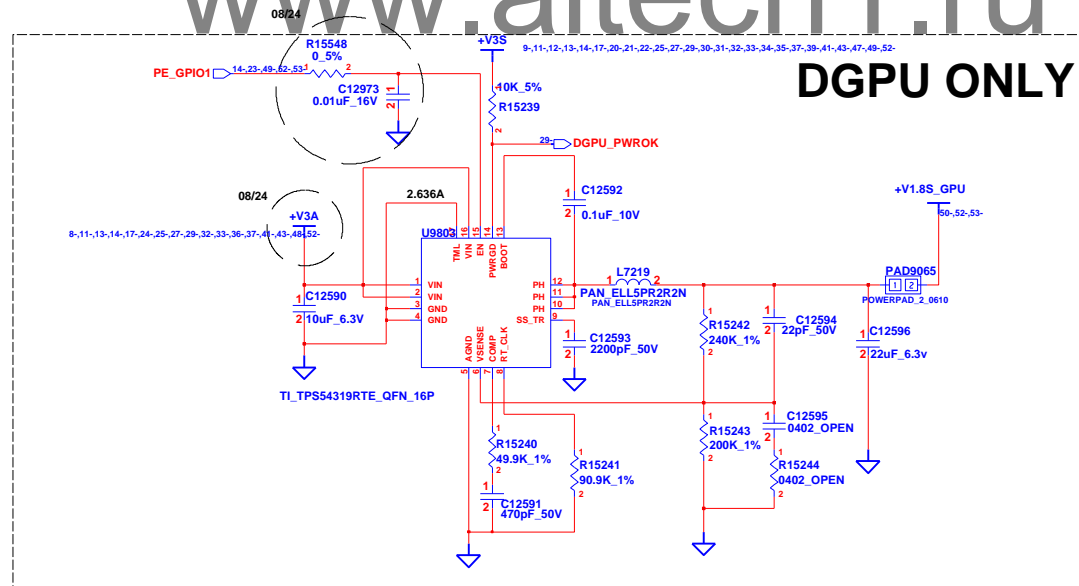
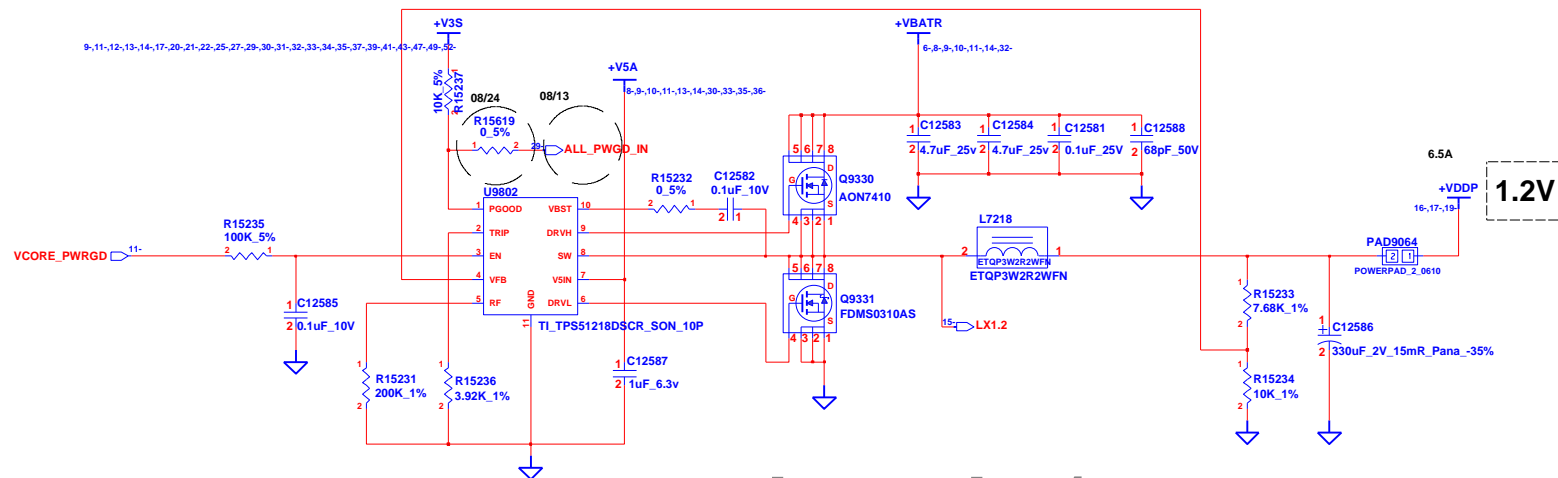
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CHANGE by Ken, Chiang 9-Jun-2010



+VDDP & +V1.8S_GPU

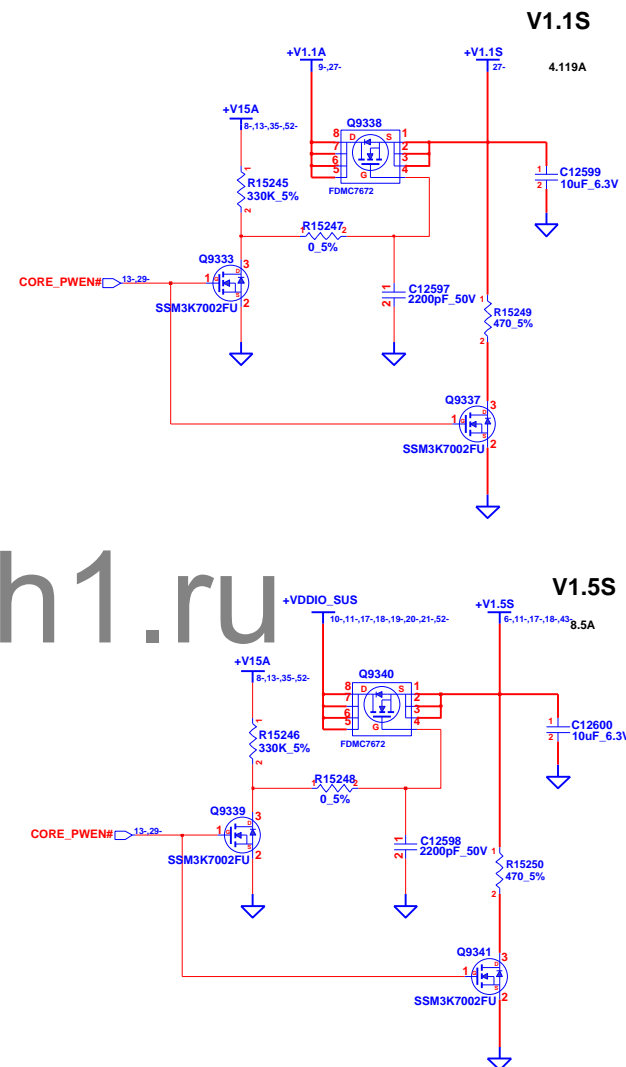
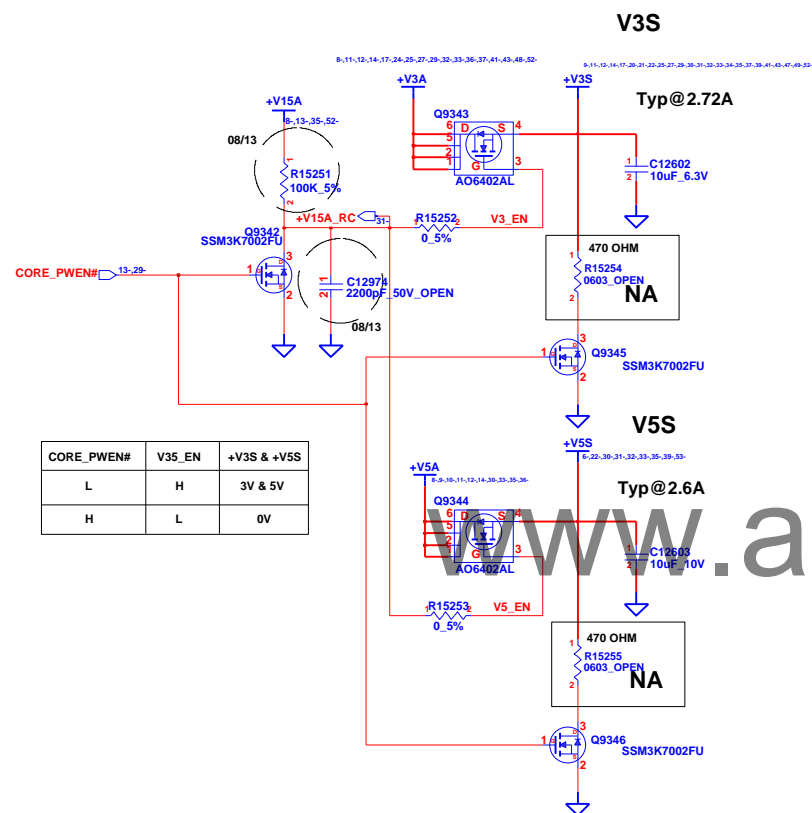


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+V5S & +V3S & +V1.5S & +V1.1S



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TITLE
ROCKY-AMD
+V5S & +V3S & +V1.5S

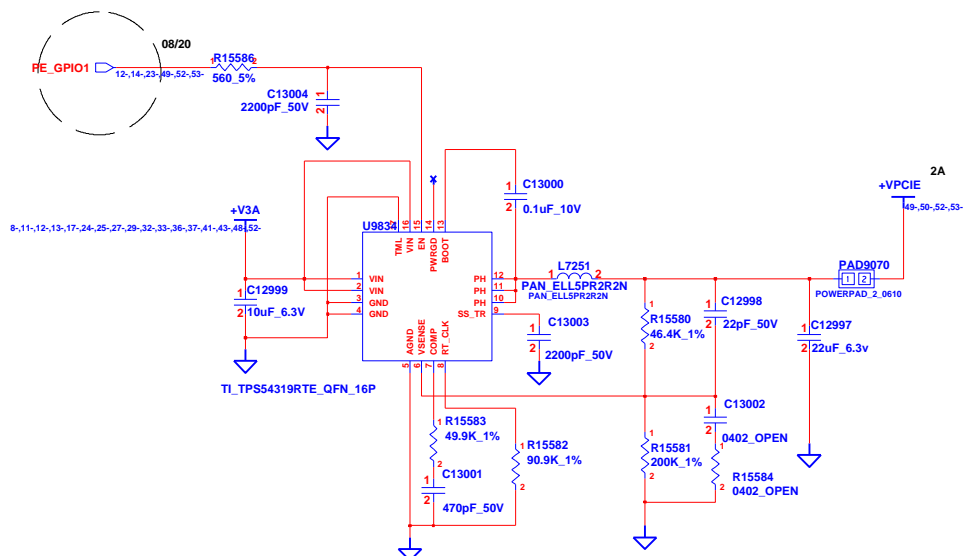
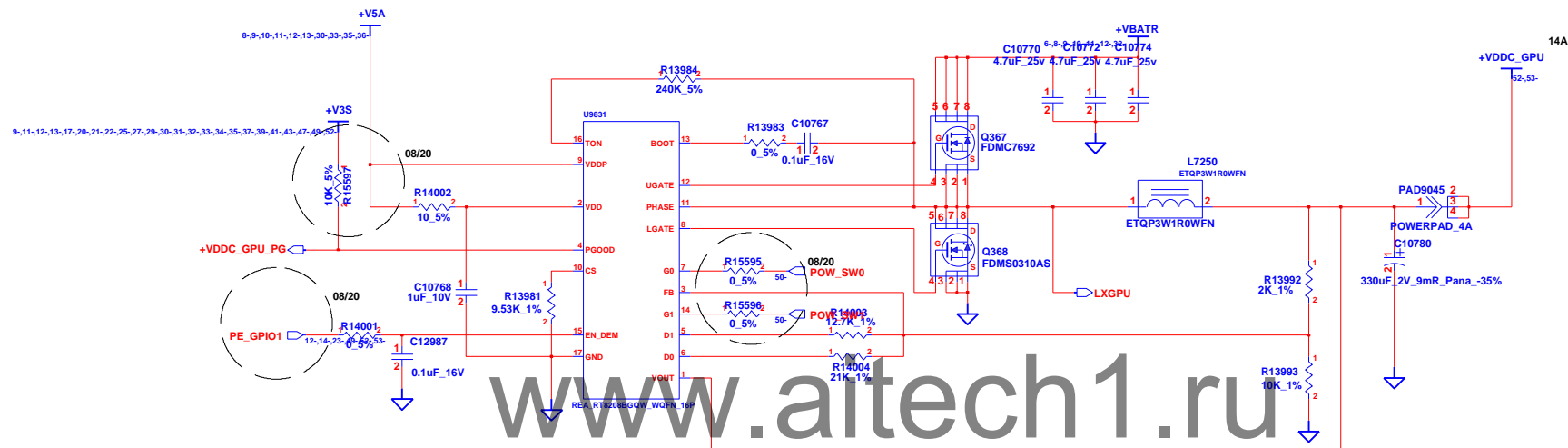
SIZE CODE CS 1234 DOC. NUMBER REV X01

CHANGE by Ken Chiang 9-Jun-2010

SHEET 13 OF 60

+VDDC_GPU & +VPCIE

POW_SW1	POW_SW0	+VDDC_GPU	Rtop	Rbot
0	0	1.1V	R50	R55 // R54
0	1	1V	R50	R55
1	0	0.95V	R50 // R91	R55 // R54
1	1	0.9V	R50 // R91	R55

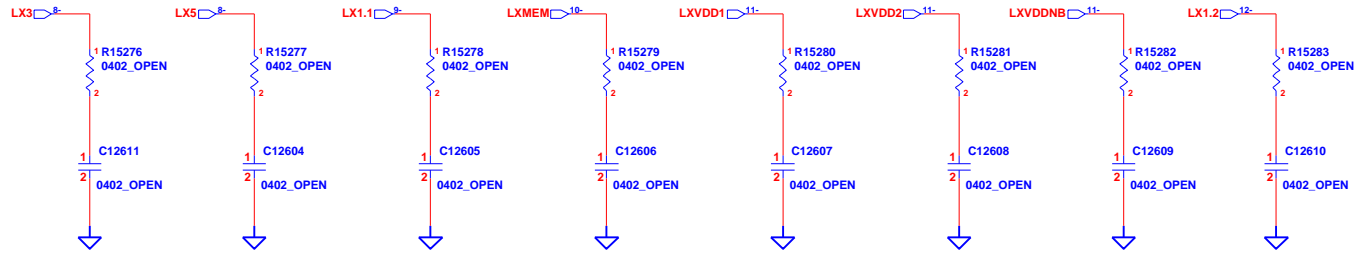


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TITLE			
ROCKY-AMD			
+VDDC_GPU & +VPCIE			
SIZE	CODE	DOC. NUMBER	REV
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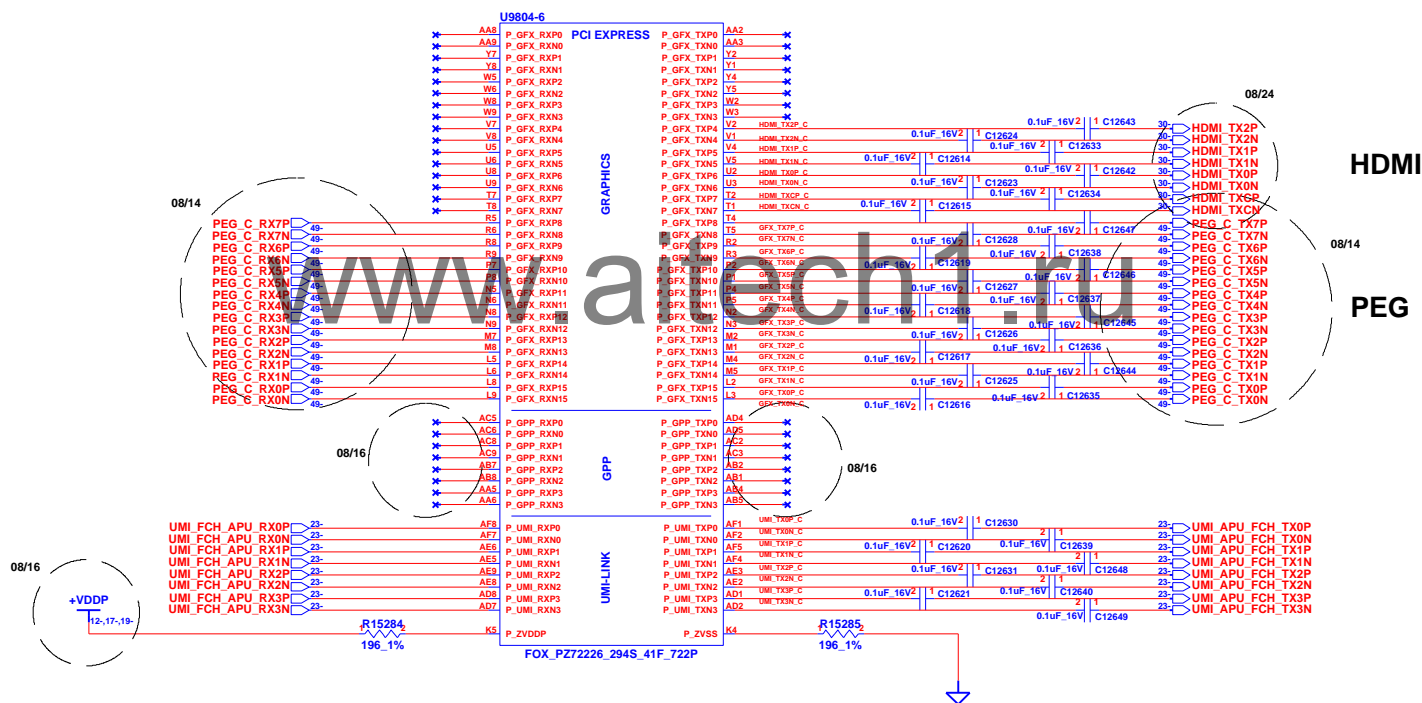


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+V1.5S_LDO

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TITLE ROCKY-AMD			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
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CPU



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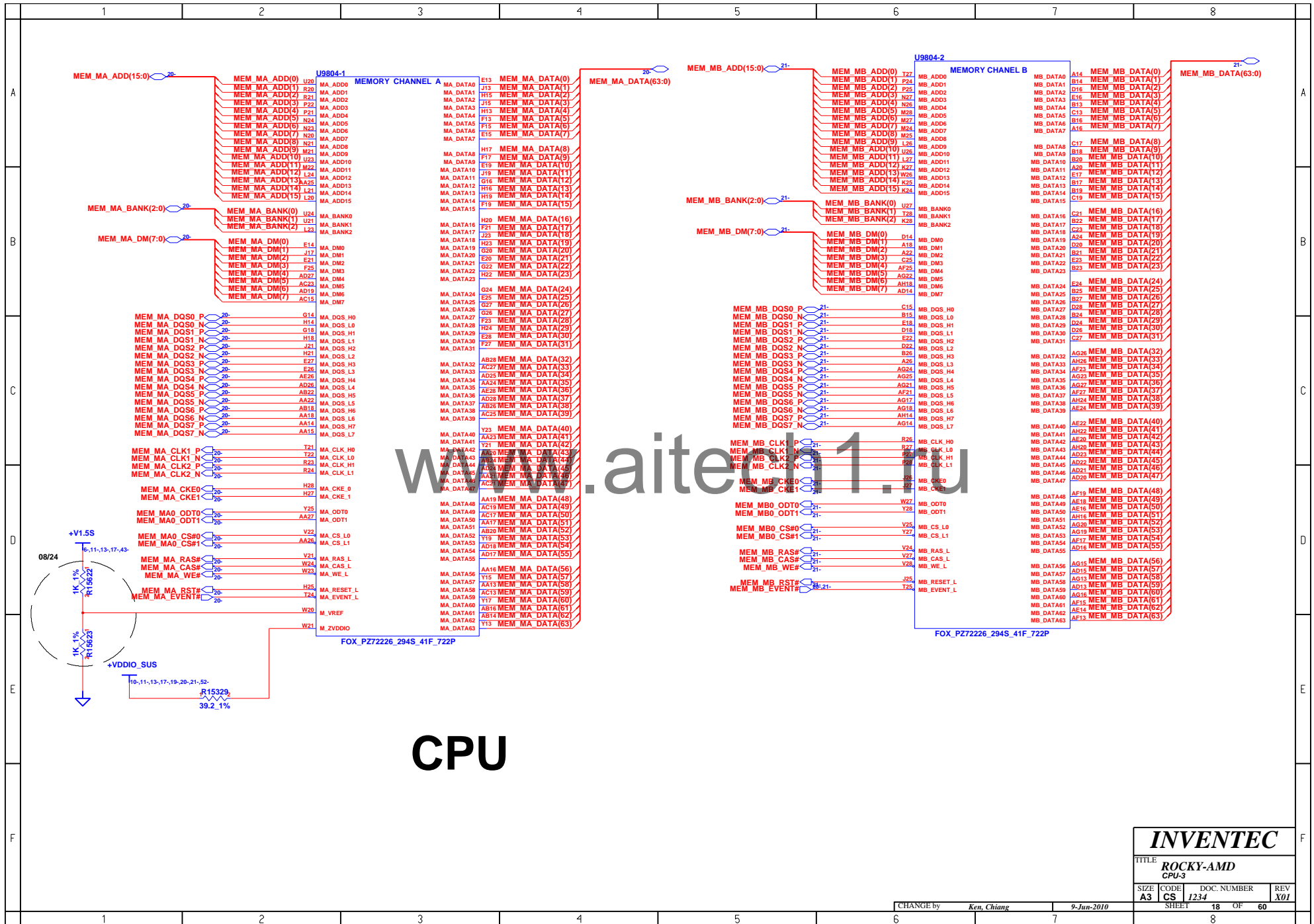
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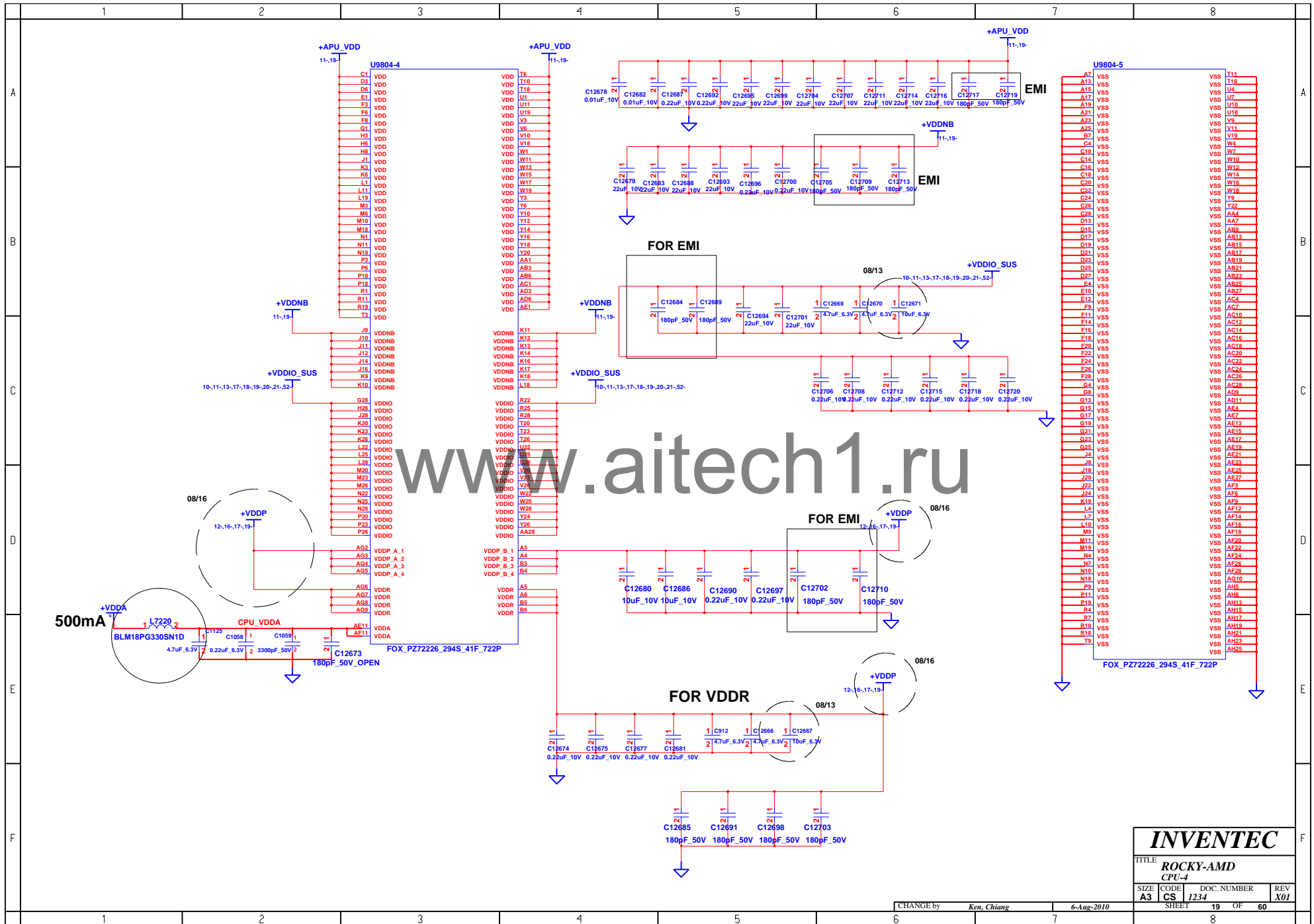
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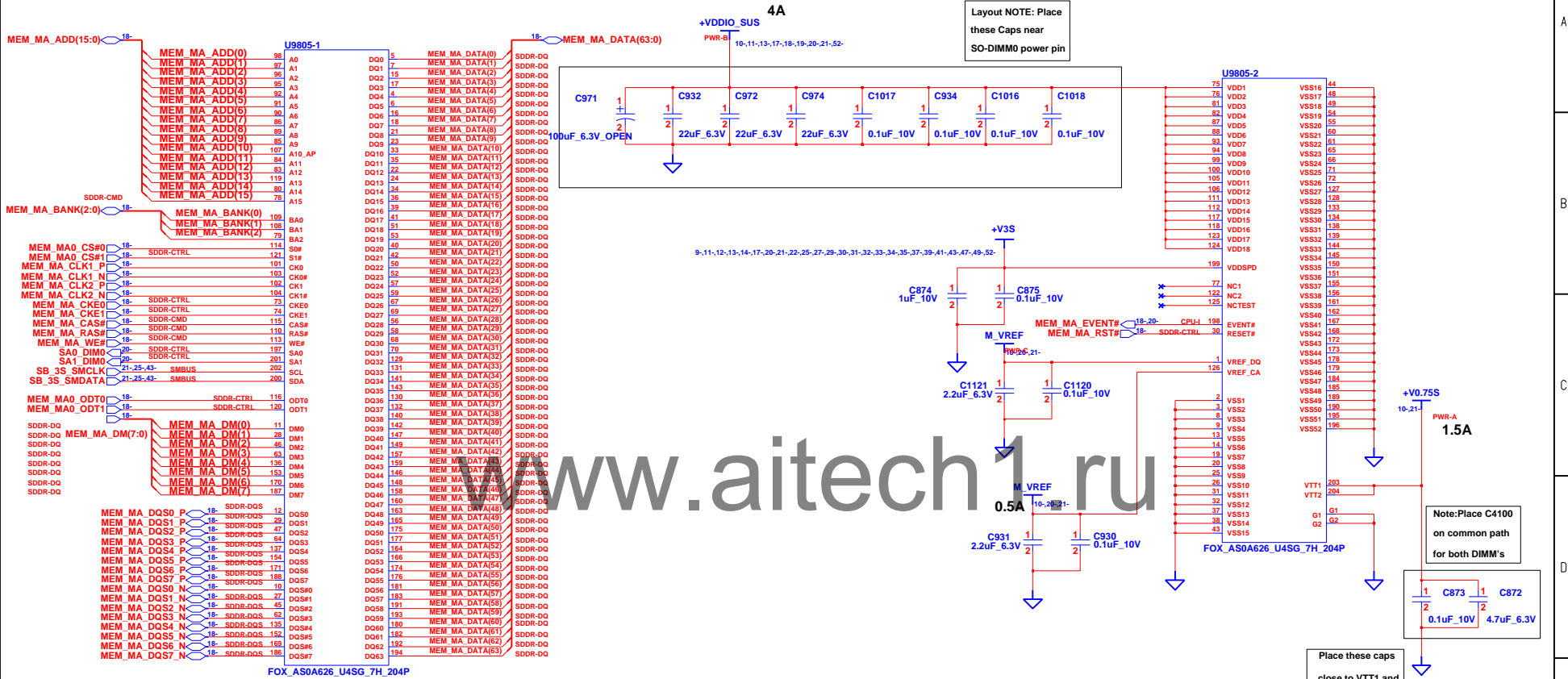
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SO-DIMM0

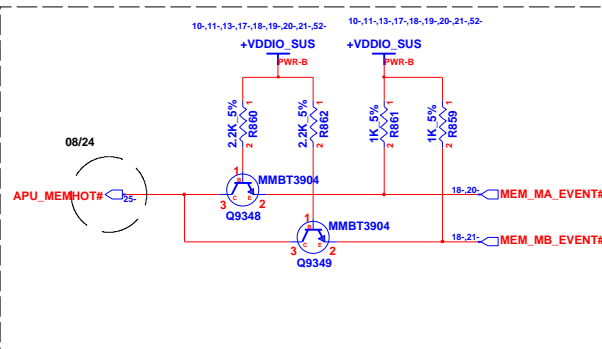


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NOTE:

IF SA0_DIM0=0, SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0x30
SO-DIMMA TS ADDRESS IS 0x30

IF SA0_DIM0=1, SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0x32
SO-DIMMA TS ADDRESS IS 0x32



INVENTEC

TITLE
**ROCKY-AMD
SO-DIMM0**

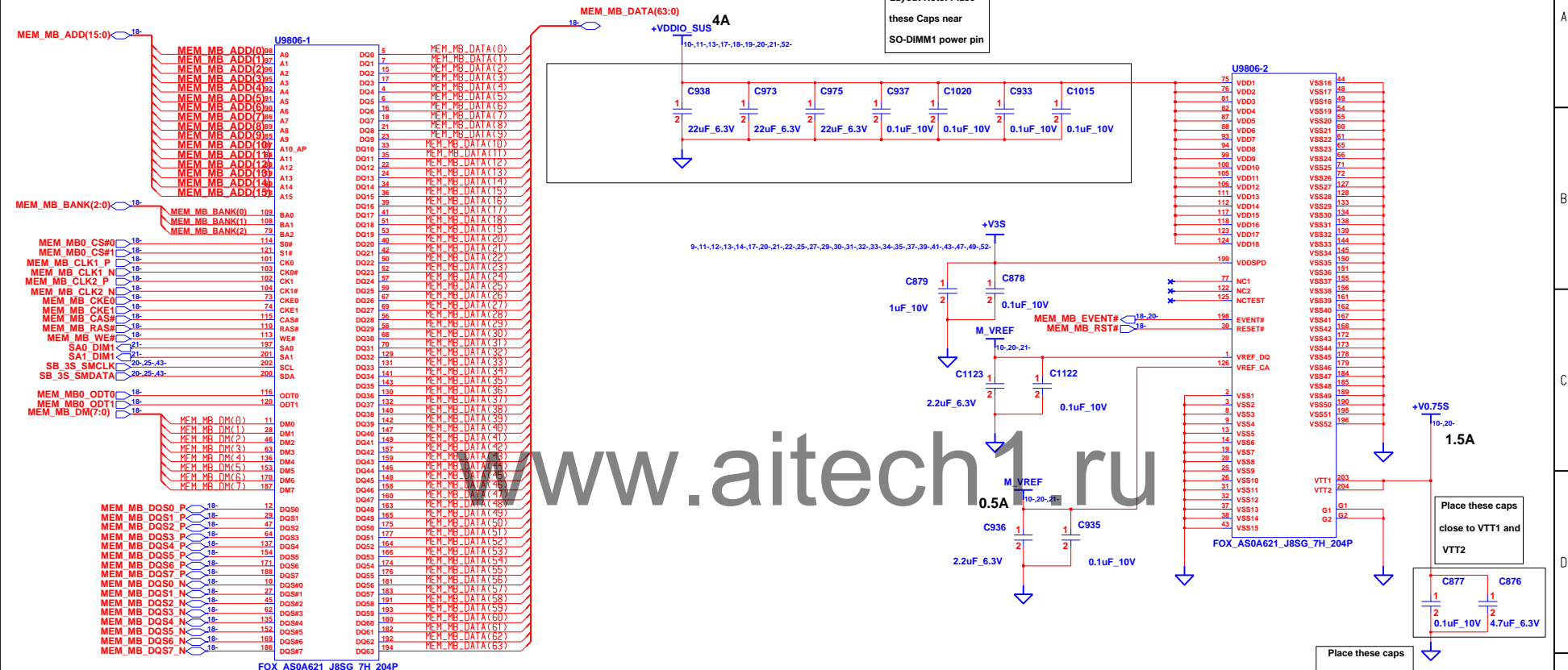
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A3	CS	1234	X01

CHANGE by **Ken, Chiang** 30-Jul-2010

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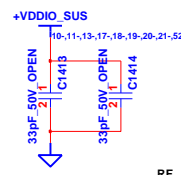
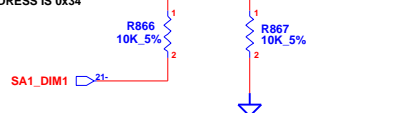
SO-DIMM1



NOTE:

SO-DIMM SPD ADDRESS IS 0xA4

SO-DIMM IS ADDRESS IS 0x34



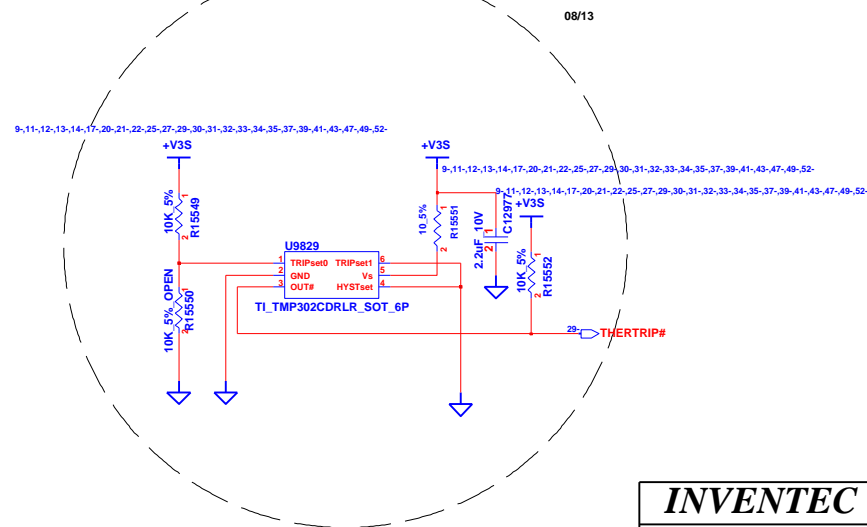
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TITLE **ROCKY-AMD**
SO-DIMMI

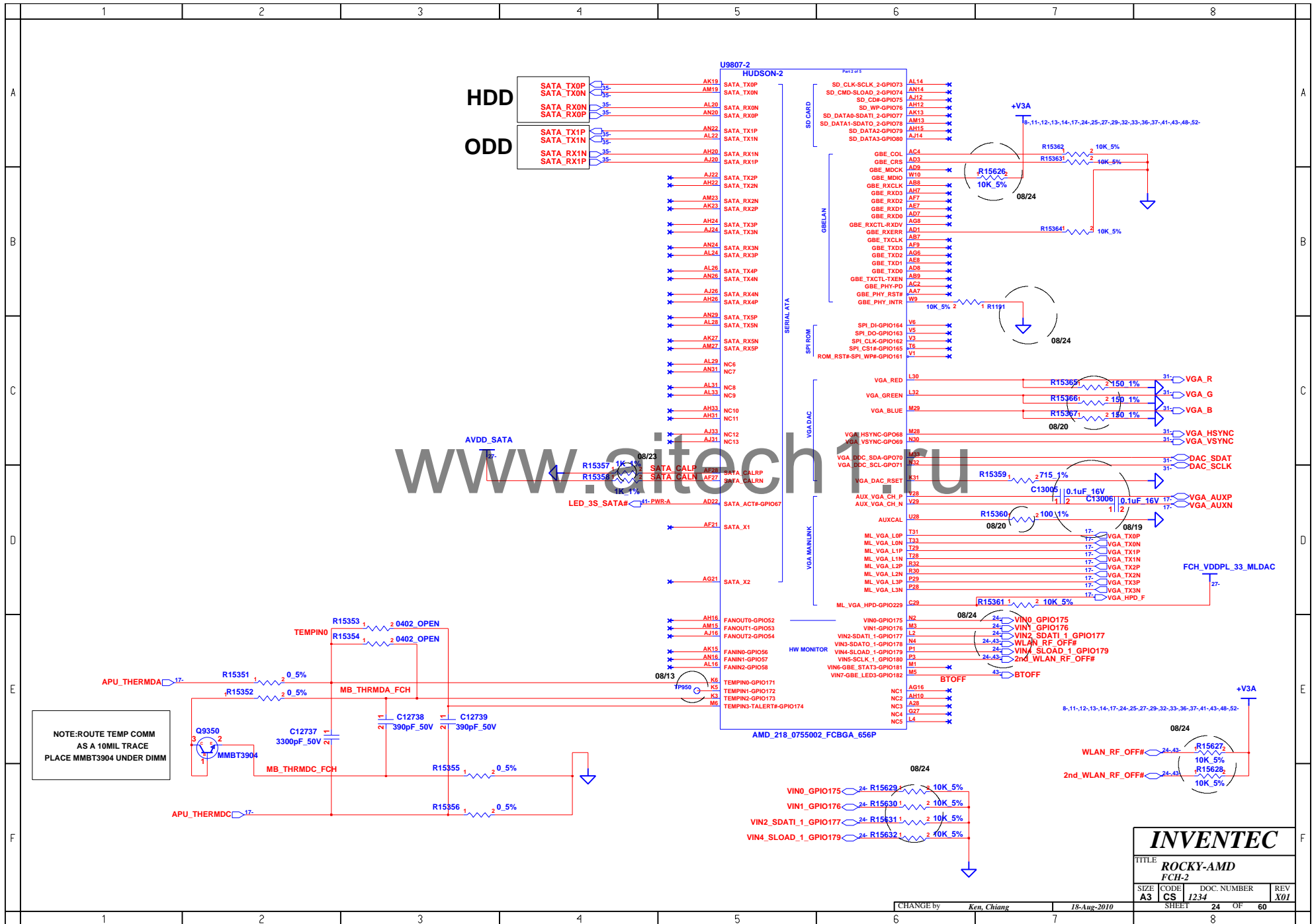
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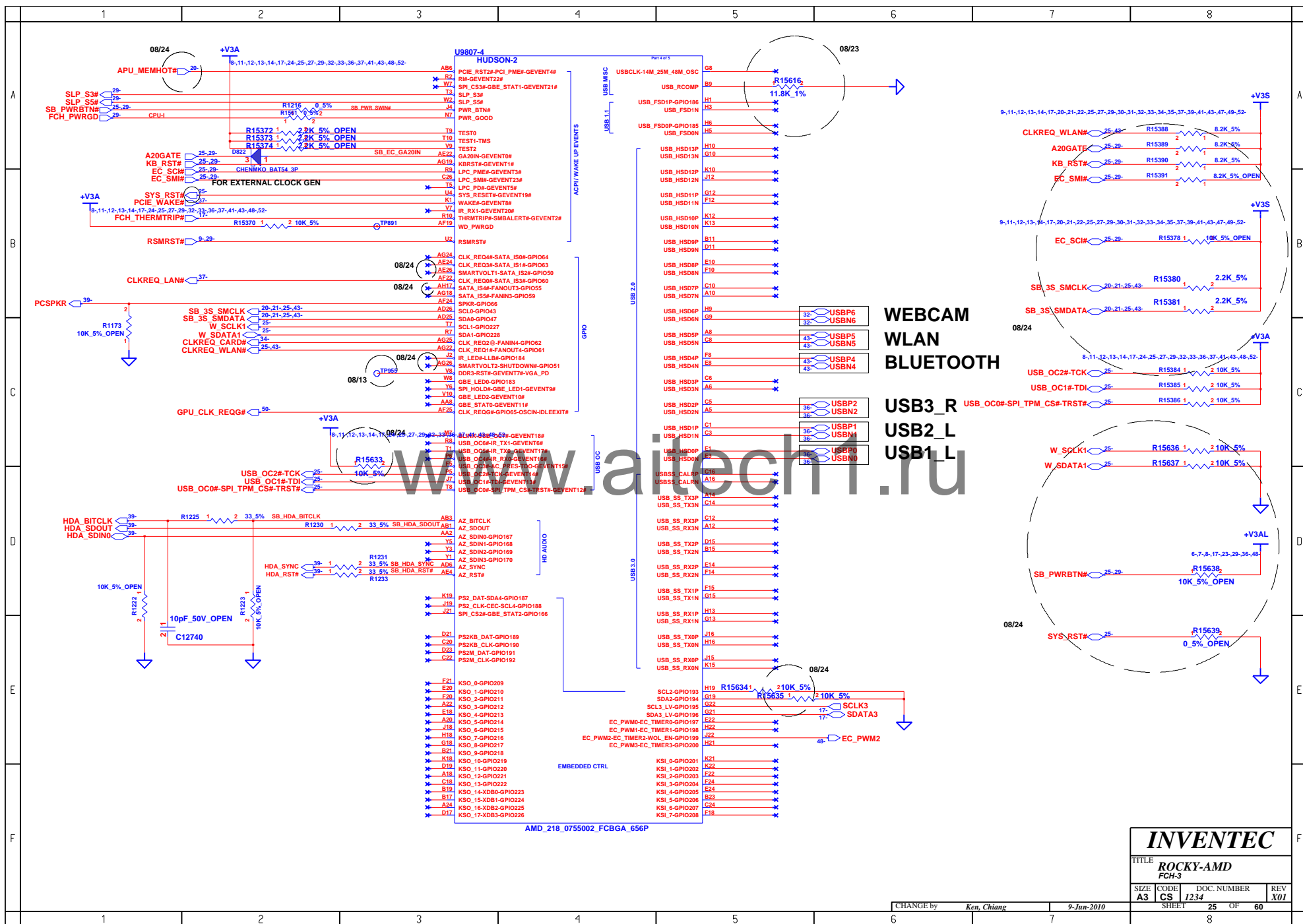
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TITLE			
ROCKY-AMD FAN & THERMAL IC			
SIZE	CODE	DOC. NUMBER	REV
A3	66		

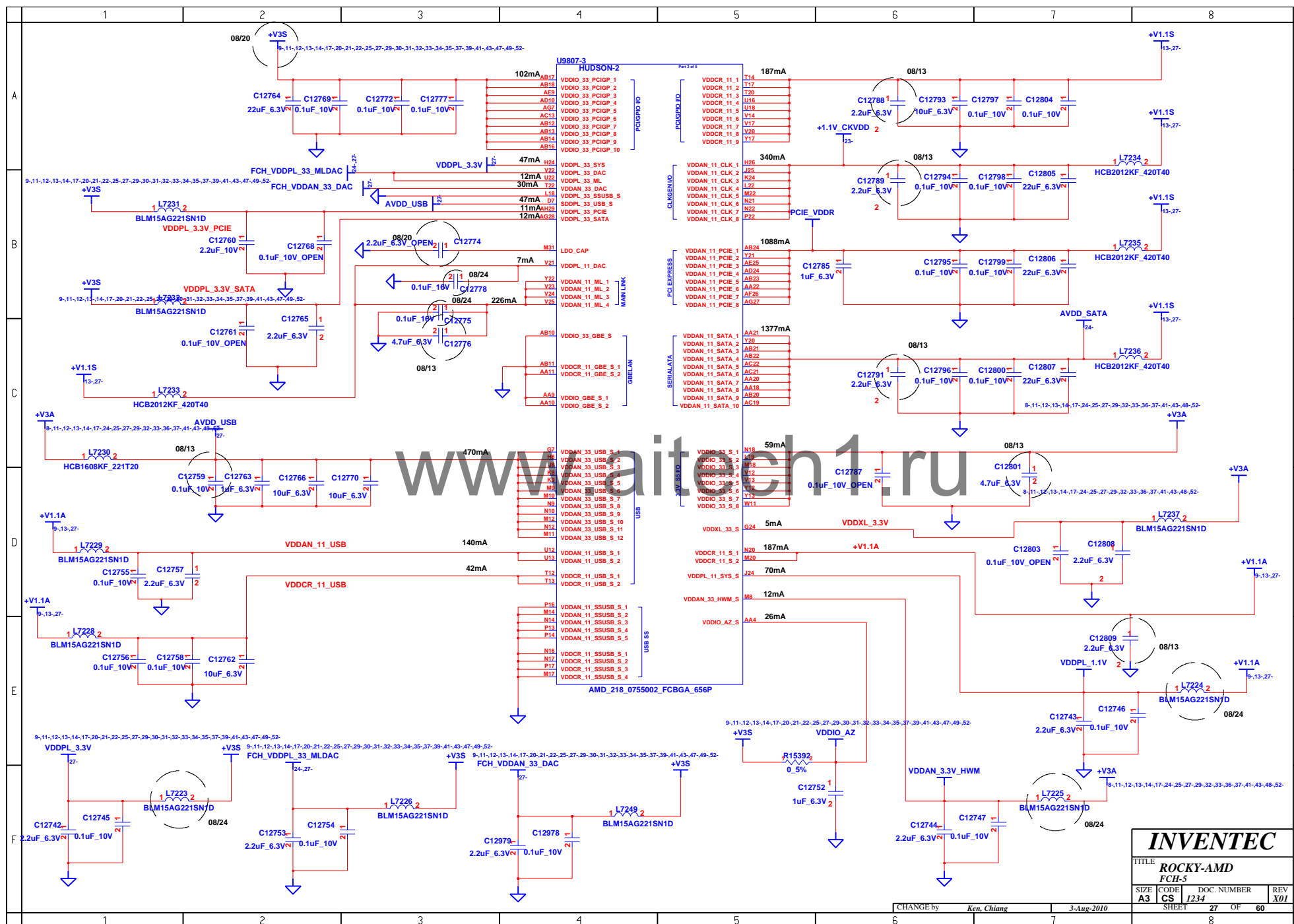


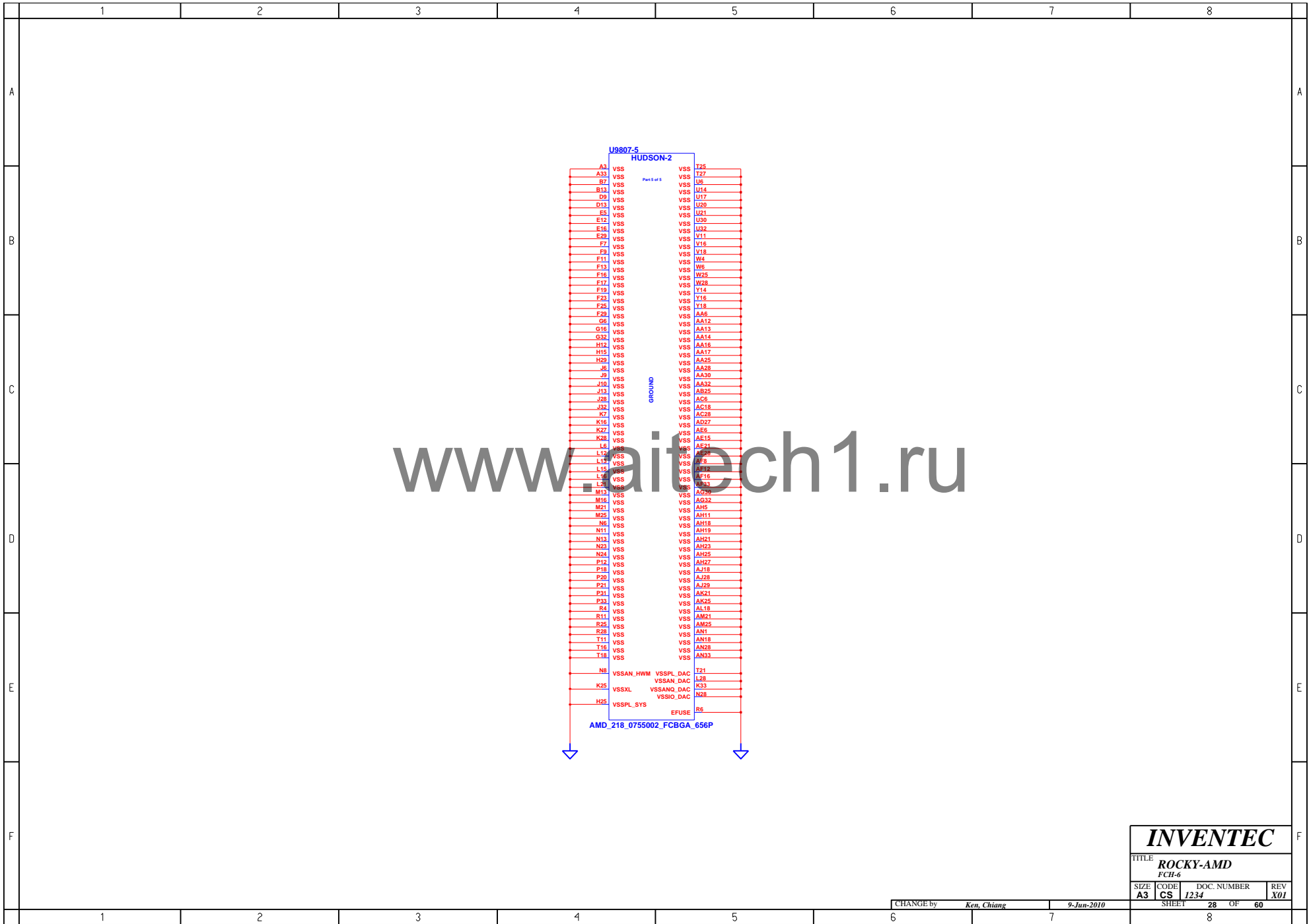


	1	2	3	4	5	6	7	8	
A									A
B									B
C									C
D									D
E									E
F									F
	1	2	3	4	5	6	7	8	

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INVENTEC			
TITLE ROCKY-AMD FCH-4			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
CHANGE by Ken, Chiang		24-Aug-2010	
SHEET		26	OF 60





INVENTEC

TITLE
ROCKY-AMD
FCH-6

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01

CHANGE by Ken, Chiang 9-Jun-2010

SHEET 28 OF 60

KBC

U805 6019B0724201

U805 ITE.IT8502E-KX-L LOFP_128P

	UMA	DIS
R12841	NA	
R12842		NA

FOR ITE 8500

SPI BIOS

BOARD ID

INVENTEC

TITLE
ROCKY-AMD
KBC

SIZE CODE DOC. NUMBER REV
A3 CS 1234 29 OF 60 X01

CHANGE by Ken Chiang

9-Jun-2010

8

HDMI

HDMI

HDMI CONN

UMA 750_1% (6013A0023301)
M92 499_1% (6013A0076801)

HDMI_TX0P 16-
HDMI_TX0N 16-
HDMI_TX1P 16-
HDMI_TX1N 16-
HDMI_TX2P 16-
HDMI_TX2N 16-
HDMI_TXCP 16-
HDMI_TXCN 16-

+V5A
I = 55mA
USB.C
C1166 1uF_10V
CLOSE TO CONNECTOR

HDMI_AUXP_CN 30-
HDMI_AUXN_CN 30-
HDMI_HPD_CN 17-

+VSS
U9835
PHP_PRT5V0U2X_SOT143_4P_OPEN
08/24

+VSS
D821 CHENMKO_BAV99_OPEN

+V3S
R1118 100K_5%
Q831 SSM3K7002FU
R15403 604_1%
R15404 604_1%
R15405 604_1%
R15406 604_1%
R15407 604_1%
R15408 604_1%
R15409 604_1%
R15411 604_1%
R1143 4.7K_5%
R1142 4.7K_5%

+VSS
D820 BAT54A

+HDMI_VDD2
FUSE801 1A_32V_0603SFF100F
SUYIN_100042MR019S1722L_19P
C1198 0.1uF_10V

DGPU_HPD_INTR

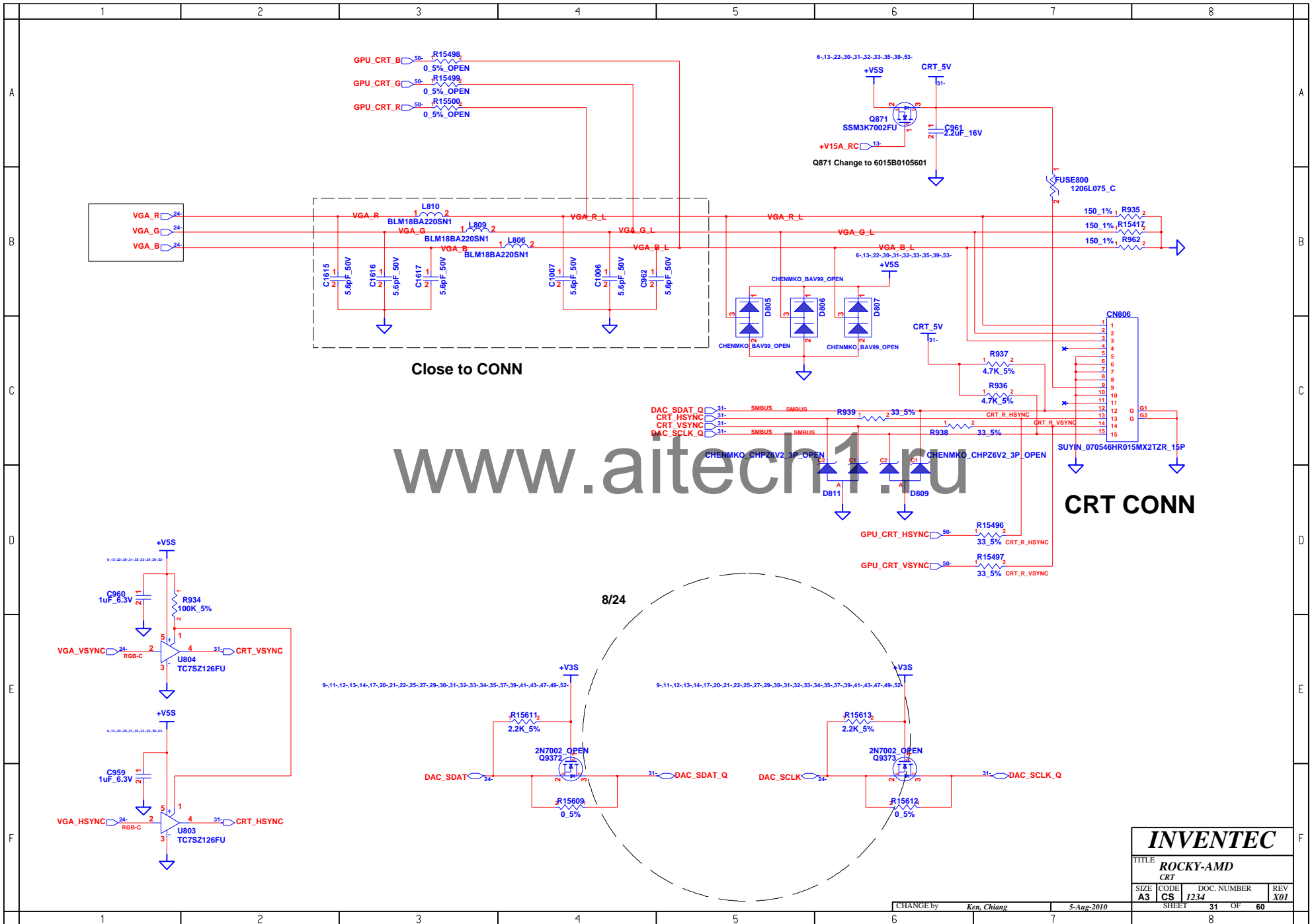
	DGPU_HPD_INTR
Plug Cable	H
Unplug Cable	L

8/14
+VSS
R15410 2.2K_5%
2N7002 Q9353
R15412 0.5%_OPEN

8/14
+VSS
R15414 2.2K_5%
2N7002 Q9354
R15415 0.5%_OPEN

INVENTEC
ROCKY-AMD
HDMI
SIZE A3
CODE CS
DOC. NUMBER 1234
REV X01
SHEET 30 OF 60

CHANGE by Ken, Chiang 9-Jun-2010



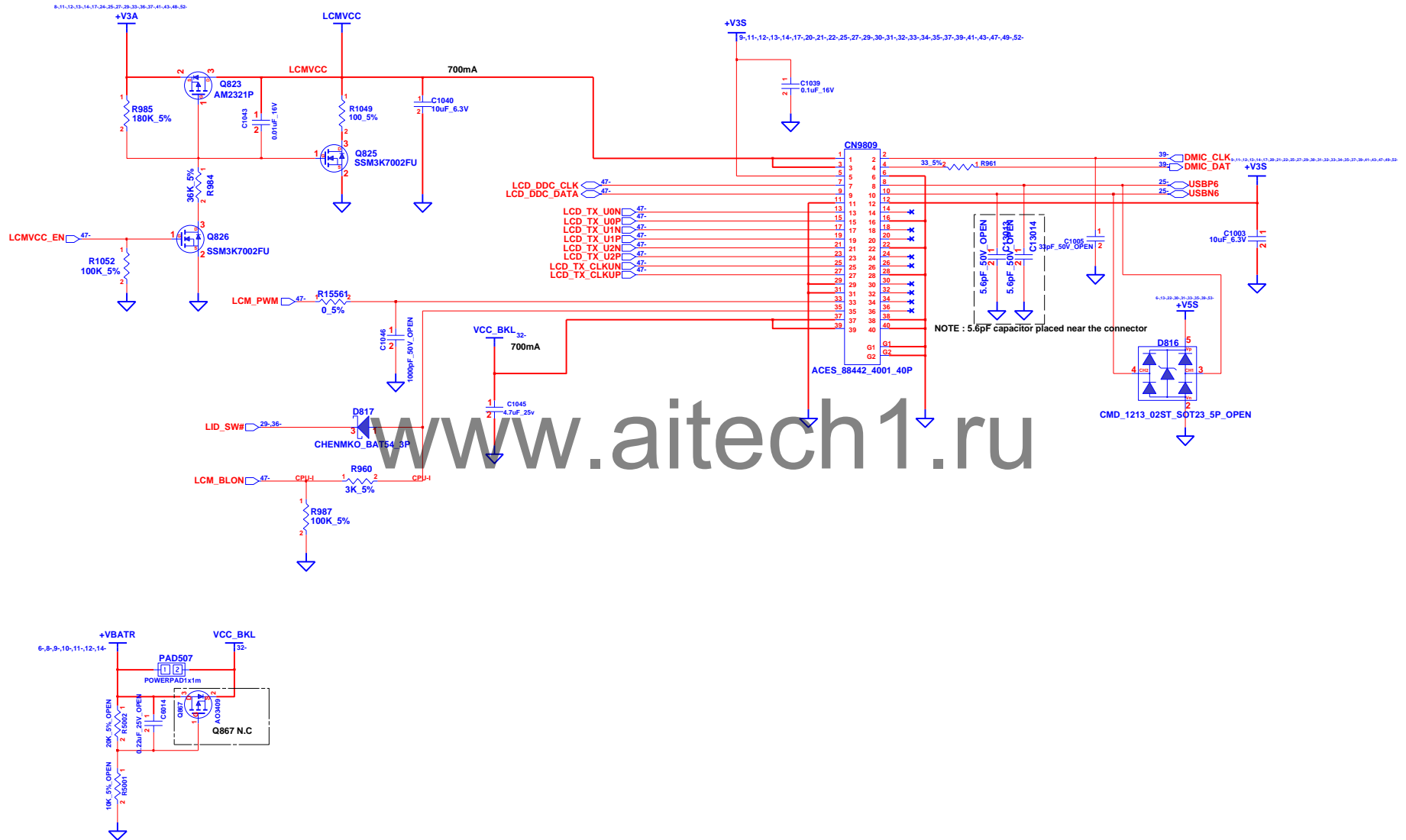
INVENTEC

TITLE
ROCKY-AMD
CRT

SIZE CODE DOC. NUMBER REV
A3 CS 1234 31 OF 60 **X01**

CHANGE by **Ken Chiang** 5-Aug-2010

LVDS



INVENTEC

TITLE
ROCKY-AMD
LVDS

SIZE CODE DOC. NUMBER REV

A3 CS 9-AUG-2010

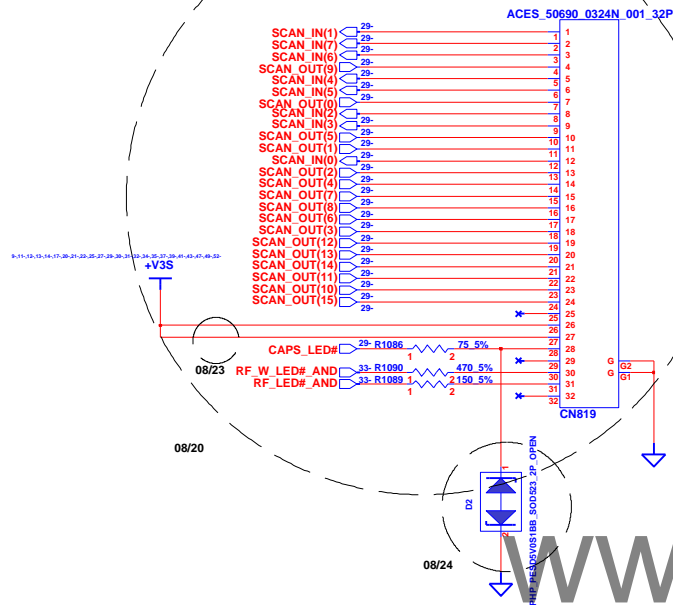
SHEET 32 OF 60

CHANGE by RKY15SB

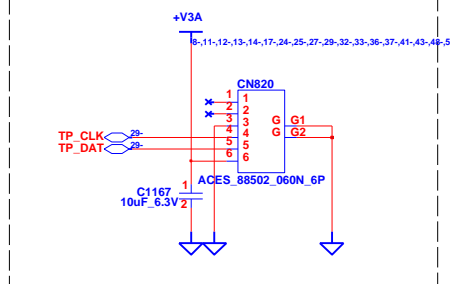
7

8

KeyBoard CONN (32 pin)



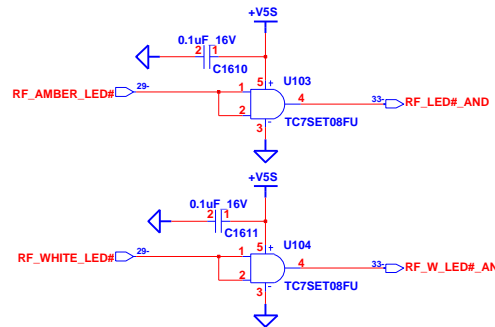
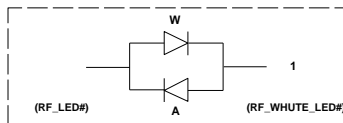
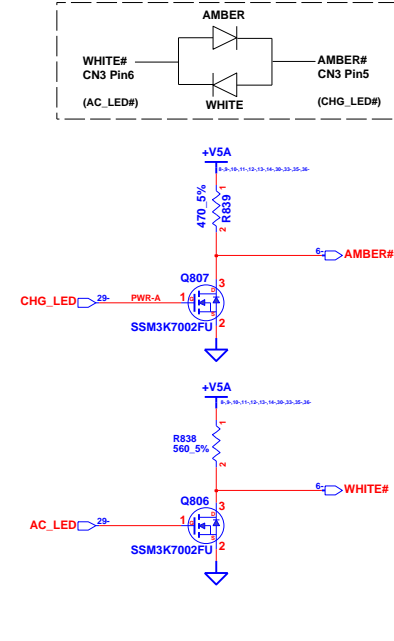
TouchPad on MB



TouchPad LED



DC-JACK LED

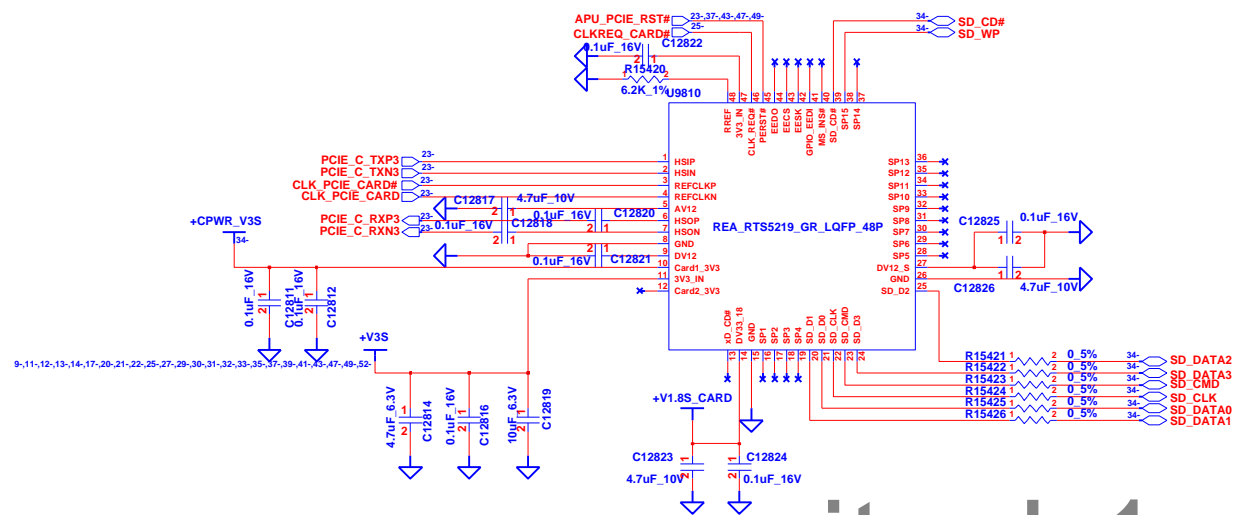


INVENTEC

TITLE			
ROCKY-AMD			
KEYBOARD CONN & Indicate LED			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01

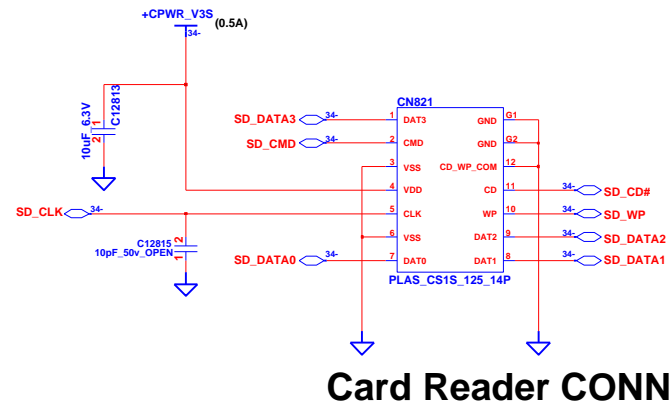
CHANGE by Ken, Chiang 5-Aug-2010

SHEET 33 OF 60



Without card	CD —	CD / WP Com
	WP —	CD / WP Com
Inserted card(unlock)	CD —	CD / WP Com
	WP —	CD / WP Com
Inserted card(lock)	CD —	CD / WP Com
	WP —	CD / WP Com

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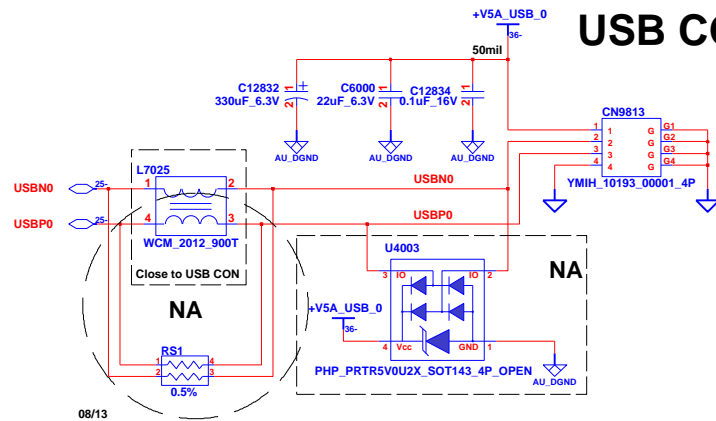
Card Reader CONN

INVENTEC			
TITLE ROCKY-AMD CARDREADER			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
SHEET 34 OF 60			

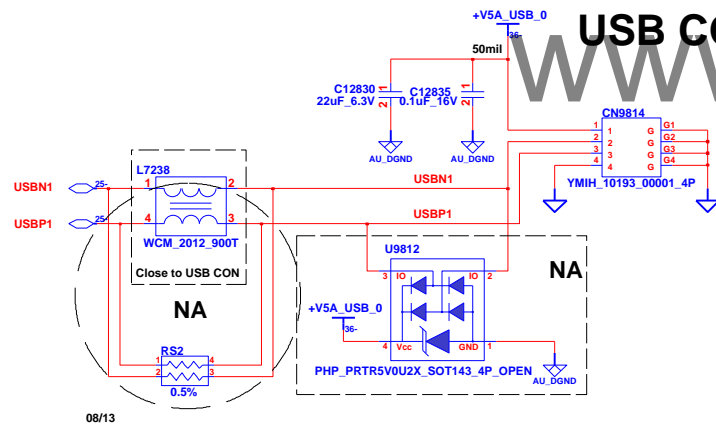
CHANGE by Ken, Chiang 5-Aug-2010

USB

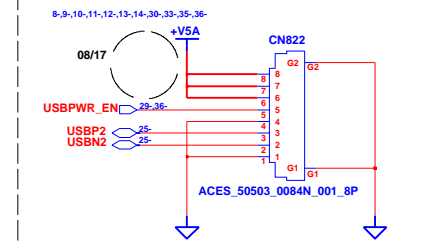
USB CONN01



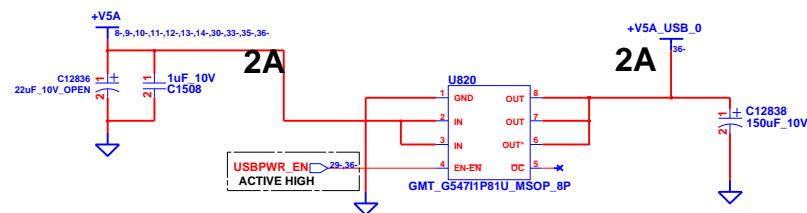
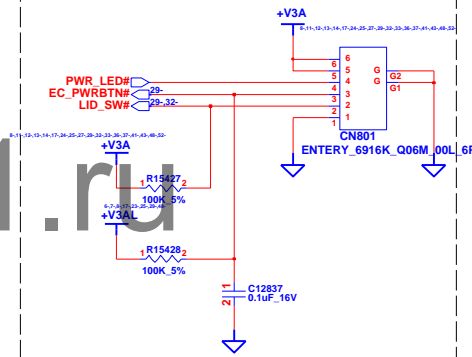
USB CONN02



USB BOARD on MB



PBN on MB



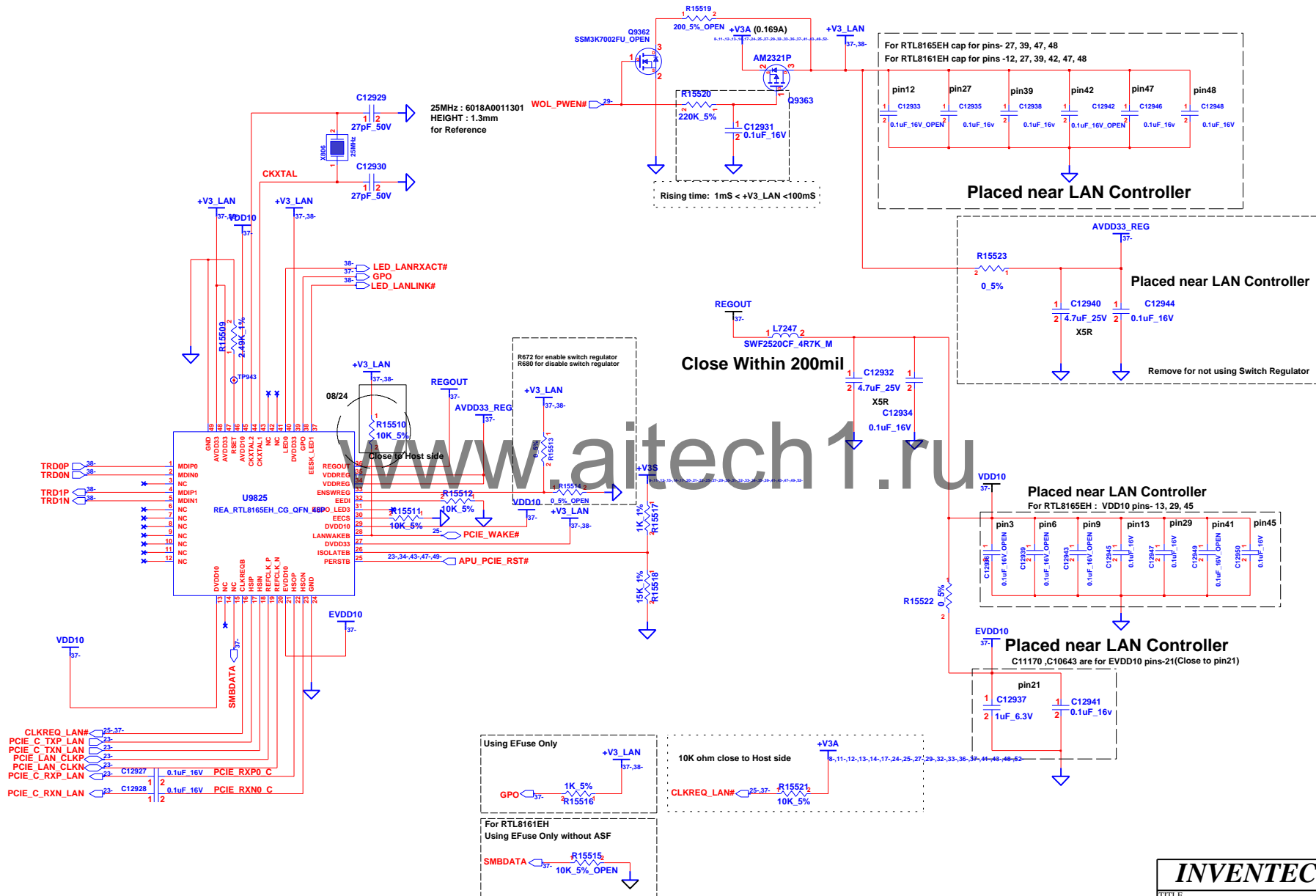
INVENTEC

TITLE			
ROCKY-AMD			
USB CONN			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01

CHANGE by Ken Chiang 5-Aug-2010

SHEET 36 OF 60

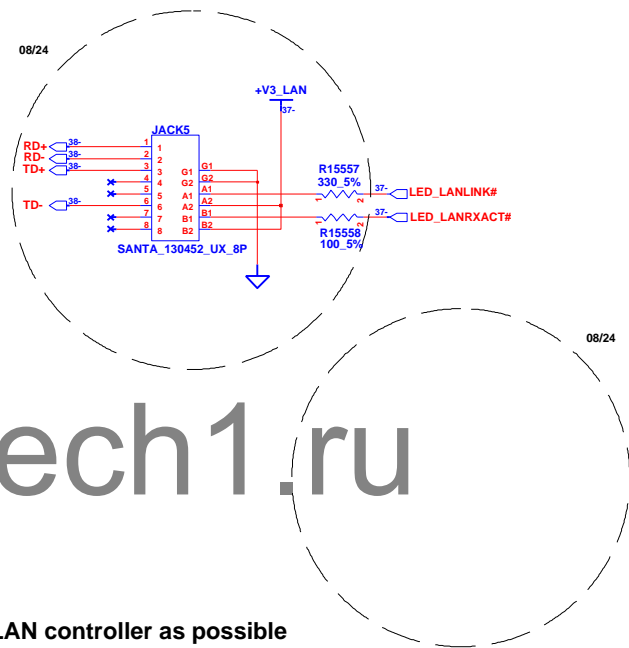
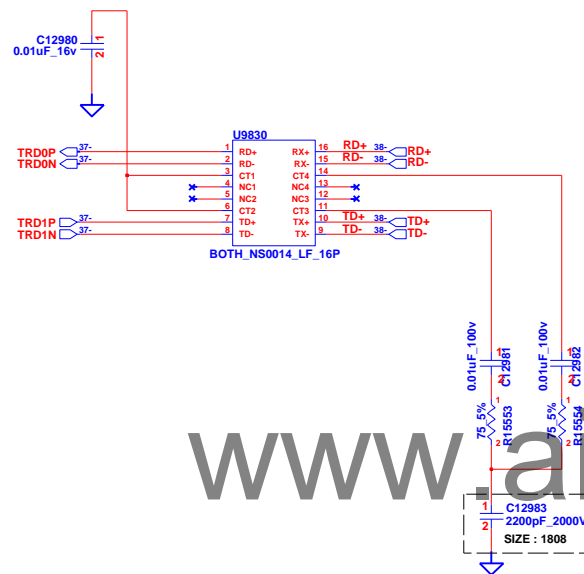
RTL8165EH 10/100LAN



INVENTEC

TITLE ROCKY-AMD LAN			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
SHEET		37	OF 60

CHANGE by Ken, Chiang 5-Aug-2010



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LAYOUT NOTE : Place termination resistors and caps as close to LAN controller as possible

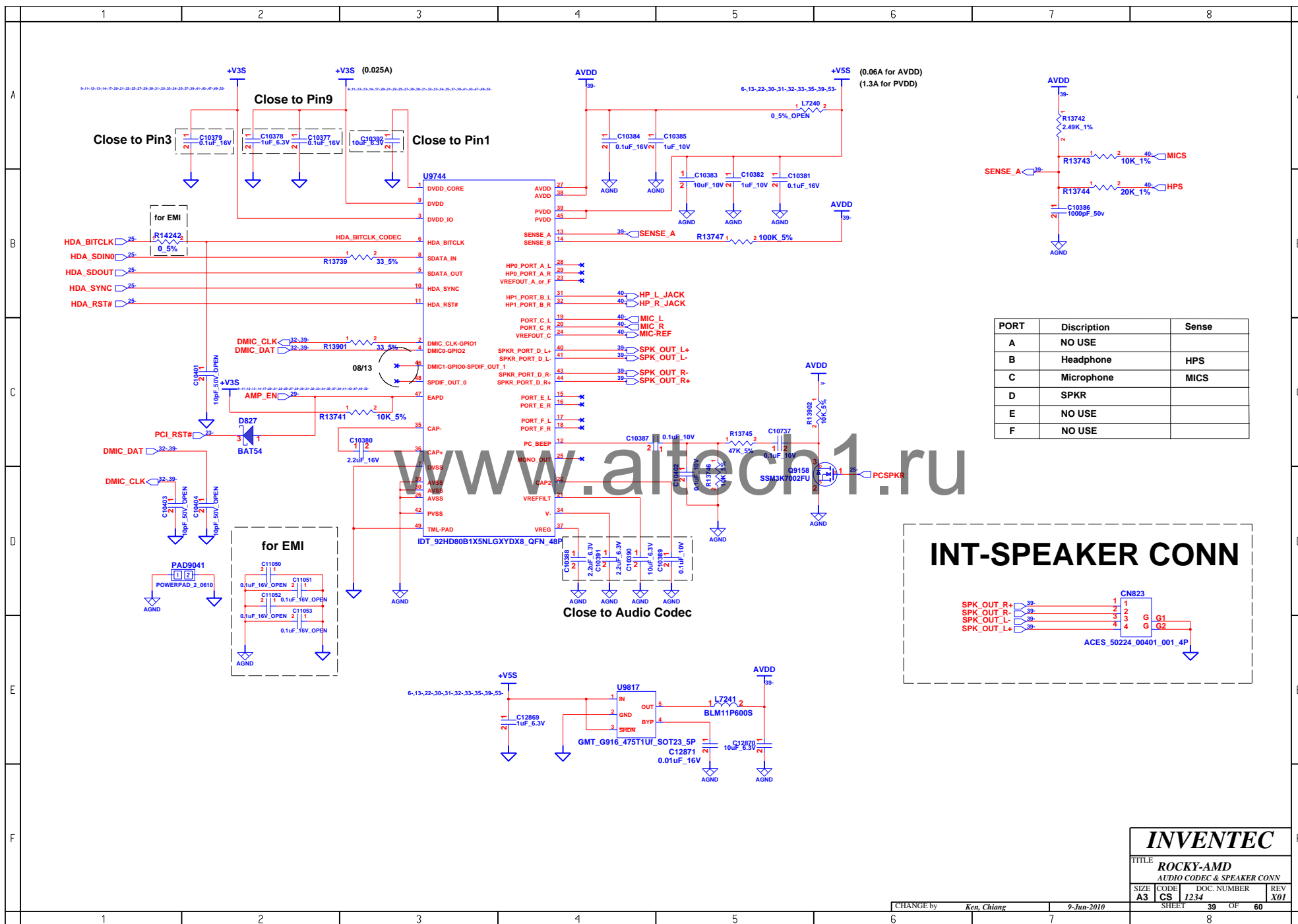
INVENTEC

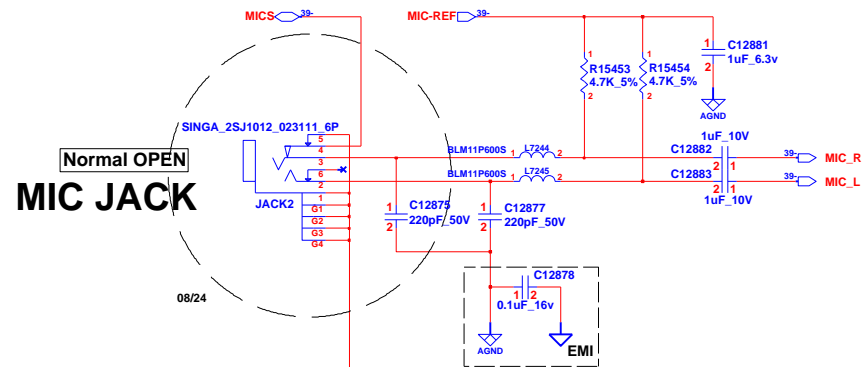
TITLE
ROCKY-AMD
RJ45 CONN

SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
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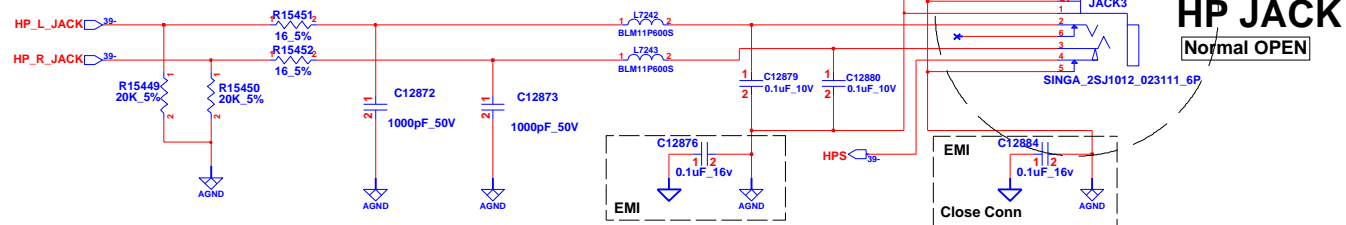
CHANGE by **Ken, Chiang** 5-Aug-2010

SHEET **38** OF **60**





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INVENTEC

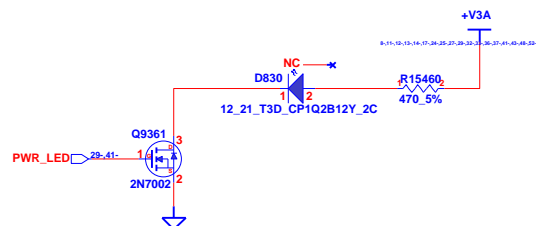
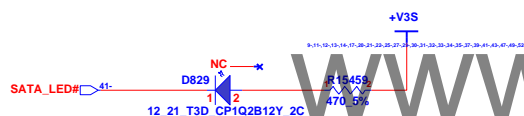
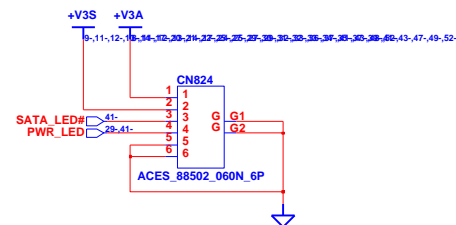
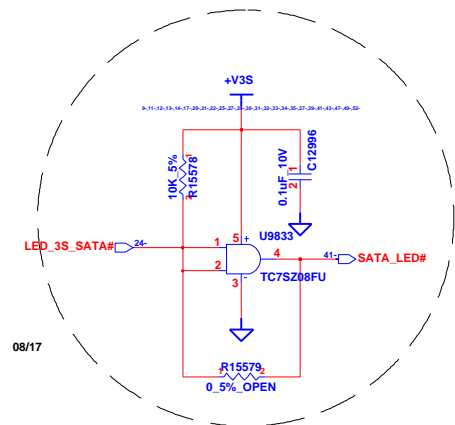
TITLE
**ROCKY-AMD
HP JACK & MIC JACK**

SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
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CHANGE by *Ken, Chiang* 9-Jun-2010

SHEET 40 OF 60

SATA LED & PWR LED



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INVENTEC

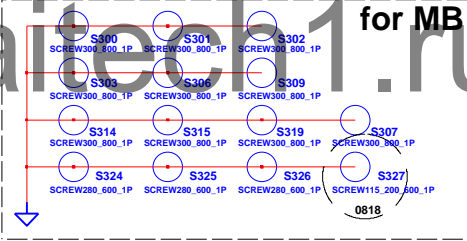
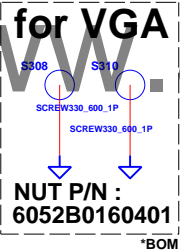
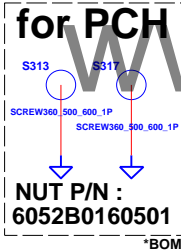
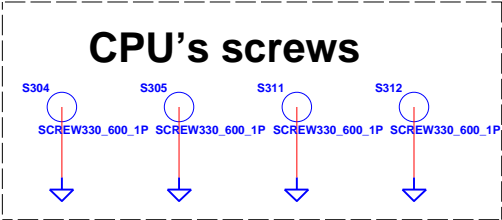
TITLE
ROCKY-AMD
SATA LED & PWR LED

SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
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CHANGE by *Ken, Chiang* 4-Aug-2010

SHEET 41 OF 60

	1	2	3	4	5	6	7	8	
A									
B									
C									
D									
E									
F									
	1	2	3	4	5	6	7	8	

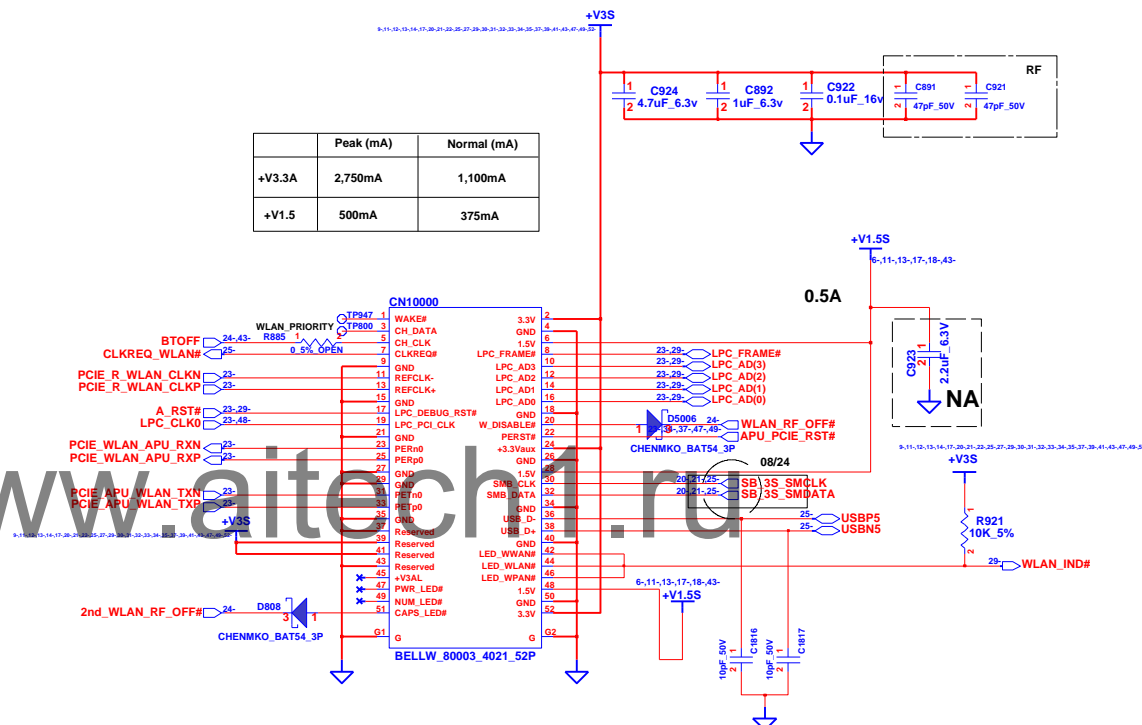


INVENTEC

TITLE ROCKY-AMD SCREW			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
SHEET		42	OF 60

CHANGE by *Ken, Chiang* 9-Jun-2010

WLAN CONN (MINICARD)



	Peak (mA)	Normal (mA)
+V3.3A	2,750mA	1,100mA
+V1.5	500mA	375mA

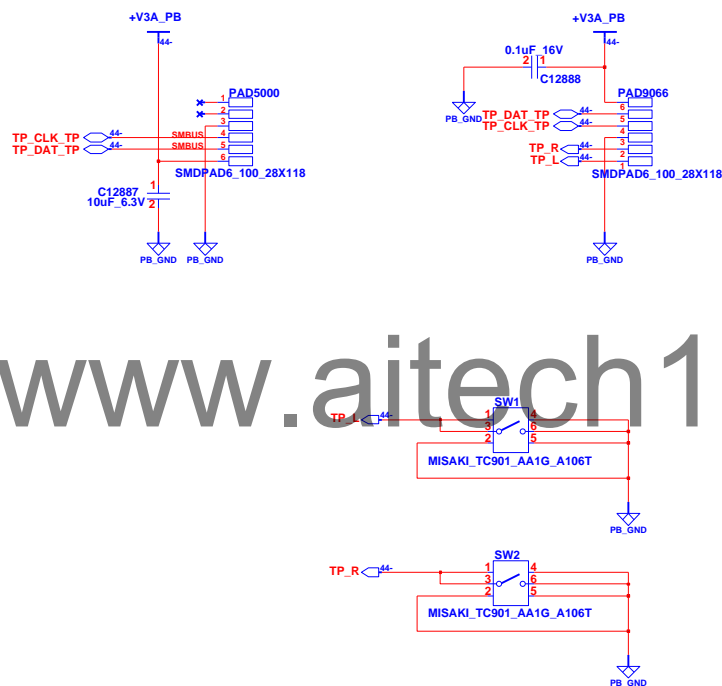
	PCH	SB800\820
WLAN_RF_OFF#	GPIO57	GPIO12
WLAN_POWER_OFF	GPIO35	GPIO176

TITLE	ROCKY-AMD WLAN & BT
-------	------------------------------------

CHANGE by	<i>Ken, Chiang</i>	<i>9-Jun-2010</i>
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CS 1234
SHEET 43 OF 60

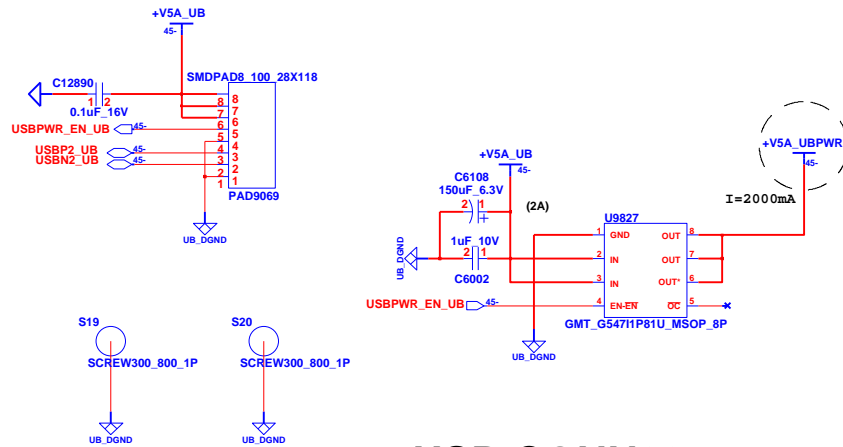
PICK BUTTON BOARD



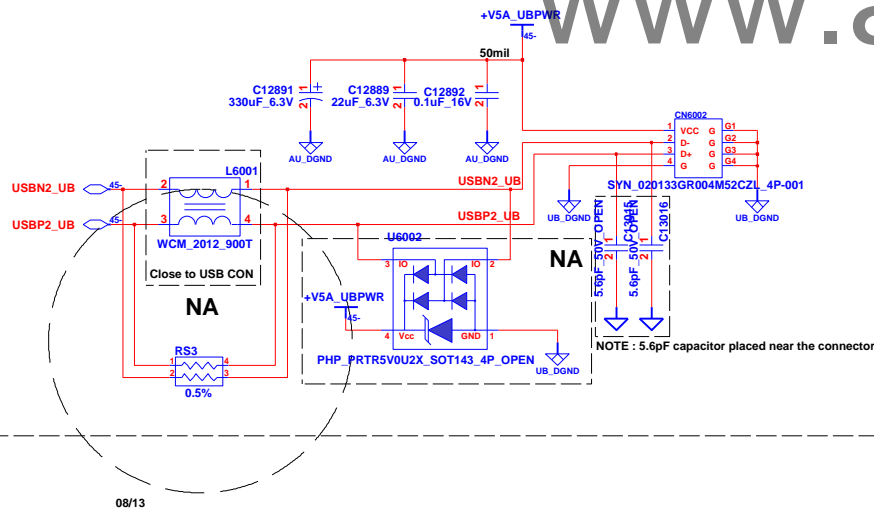
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INVENTEC			
TITLE ROCKY-AMD PICK BUTTON BOARD			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
CHANGE by Ken, Chiang		9-Jun-2010	
SHEET		44	OF 60

USB BOARD

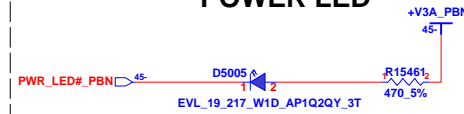


USB CONN03

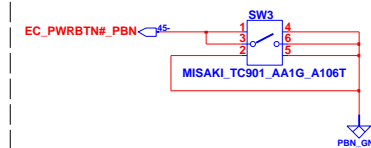


POWER BOTTON BOARD

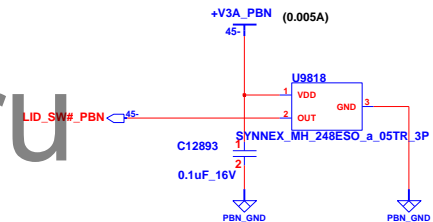
POWER LED



POWER BUTTON



LID SWITCH



INVENTEC

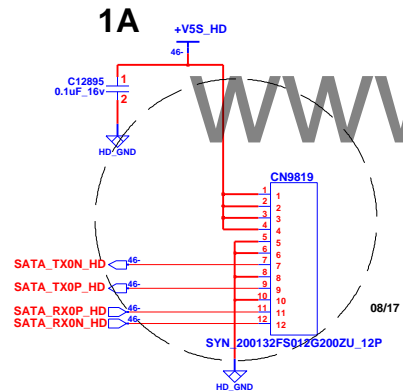
TITLE			
ROCKY-AMD			
USB/B & POWER BOTTON/B			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01

CHANGE by Ken Chiang 9-Jun-2010

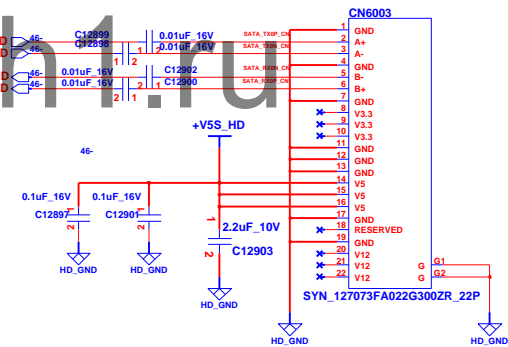
SHEET 45 OF 60

SATA HDD BOARD

SATA HDD FFC CONN on HDD/B



HDD CONN

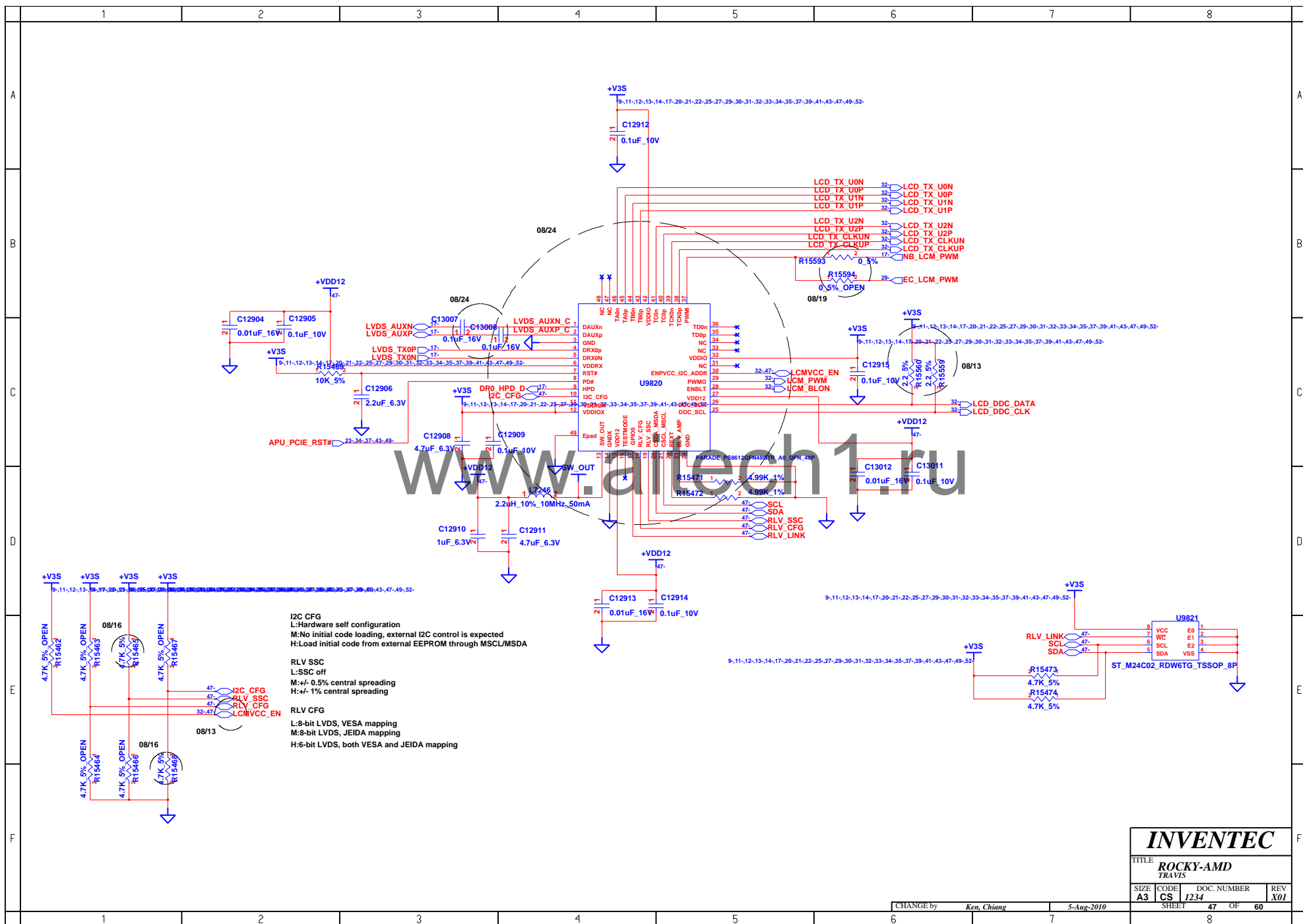


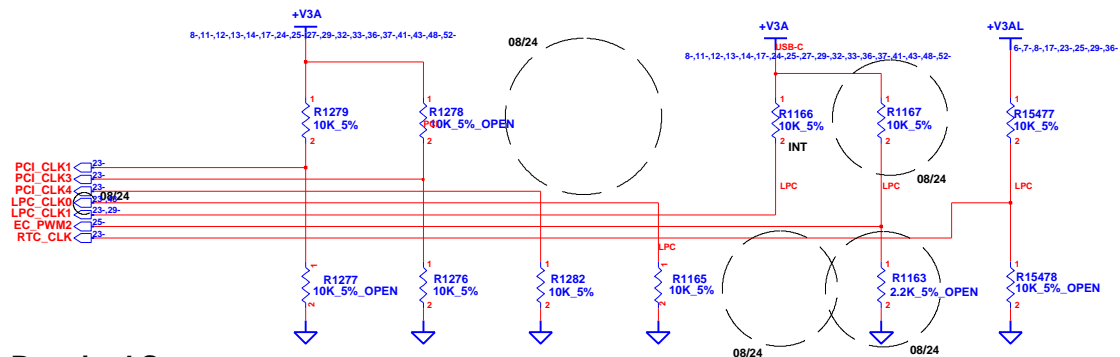
INVENTEC

TITLE			
ROCKY-AMD SATA HDD BOARD			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01

CHANGE by Ken Chiang 9-Jun-2010

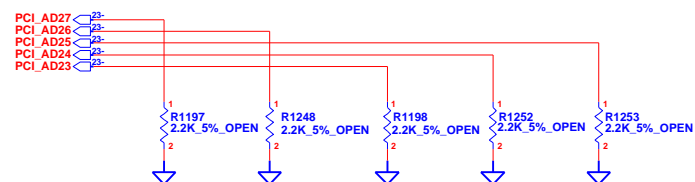
SHEET 46 OF 60





Required Straps:

RTCCCLK		PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	PCI_CLK1	EC_PWM2
S5 PLUS MODE DISABLE (DEFAULT)	PULL HIGH	ALLOW PCIe Gen2 DEFAULT	USE DEBUG STRAP	non Fusion CLOCK MODE APU_CLK AND DISP_CLK NO CLOCK OUTPUT	EC ENABLED	INTEGRATED CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT
S5 PLUS MODE ENABLE	PULL LOW	FORCE PCIe Gen1	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK MODE DEFAULT APU_CLK AND DISP_CLK CLOCK OUTPUT FROM INT CLOCK GEN	EC DISABLED DEFAULT	INTEGRATED CLKGEN DISABLED	SPI ROM

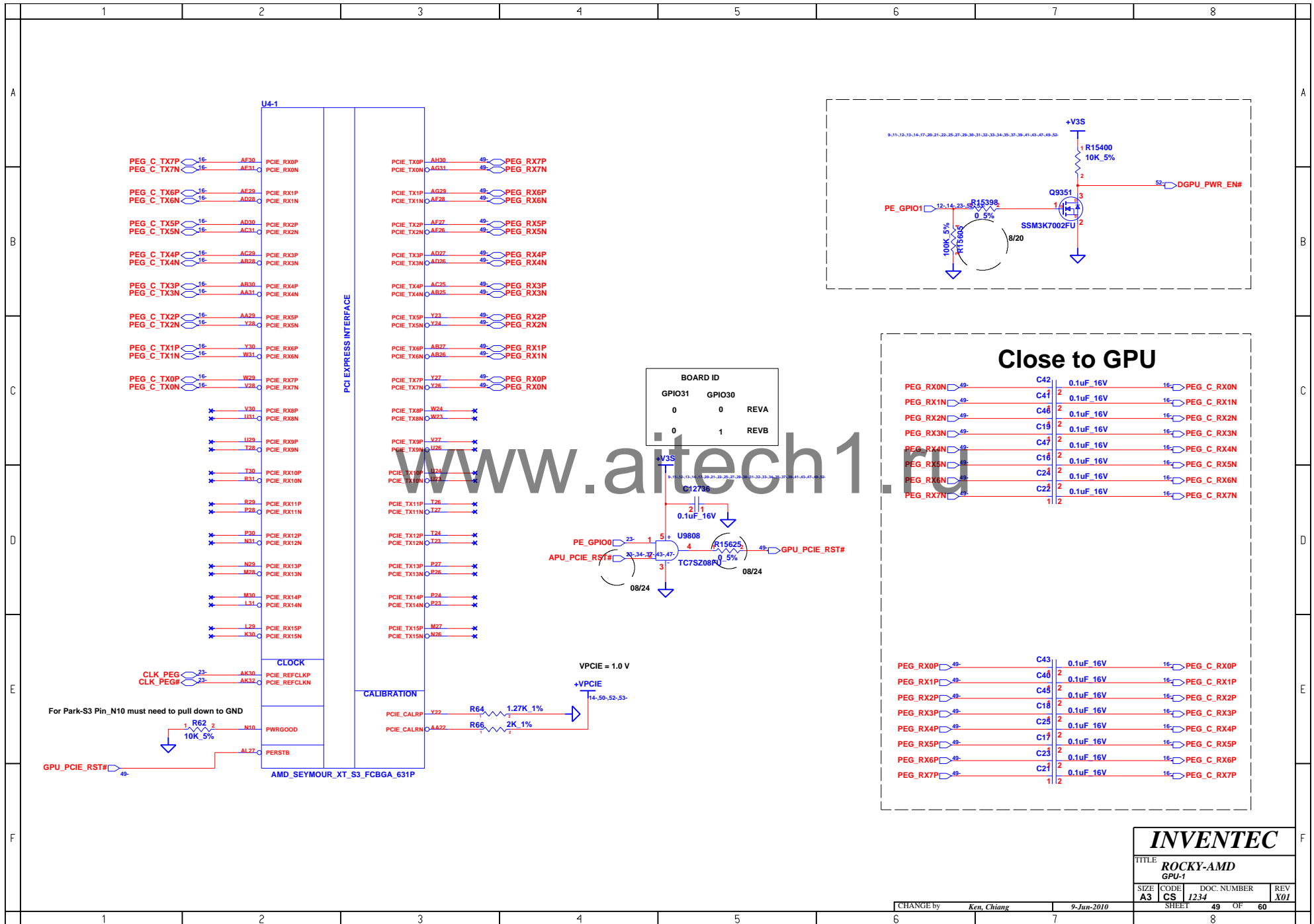


Debug Straps

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_3S_AD27	PCI_3S_AD24	PCI_3S_AD23
PULL HIGH	USE PCI PLL (default)	GETTING I2C ROM ENABLE	DISABLE PCI MEM BOOT (default)
PULL LOW	BYPASS PCI PLL	USE EEPROM PCI STRAPS I2C ROM DISABLE	ENABLE PCI MEM BOOT

INVENTEC			
TITLE ROCKY-AMD SRTAP			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
CHANGE by Ken Chiang		9-Jun-2010	
SHEET		48 OF 60	
		8	



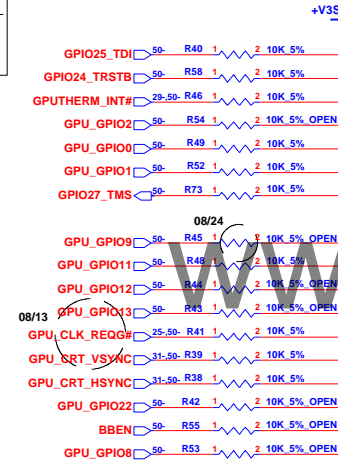
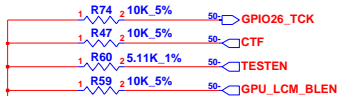
MEM_ID3 R15454	MEM_ID2 R15453	MEM_ID1 R15452	MEM_ID0 R15451	vendor
0	0	0	1	Samsung(512MB)
0	0	1	1	hynix (512MB)
0	0	0	0	Samsung(1G)
0	0	1	0	hynix (1G)
0	1	1	0	Samsung(1G) C-die

(Default)

STRAPS	PIN	Description of default settings
TX_PWRS_ENB	GPIO0	PCIe full TX output swing.
TX_DEEMPH_EN	GPIO1	PCIe transmitter de-emphasis enabled.
BIF_GEN2_EN_A	GPIO2	PCIe GEN2 enabled
BIF_DEBUG_ACCESS	GPIO4	Debug signals muxed out.
BIF_VGA_DIS	GPIO7_BLON	Control Backlight On / Off
ROMIDCFG(2:0)	GPIO9	VGA ENABLED
	GPIO[13:11]	Memory aperture size select.

If GPIO_22_EN = 0, then GPIO[13:11] defines the primary memory aperture size.

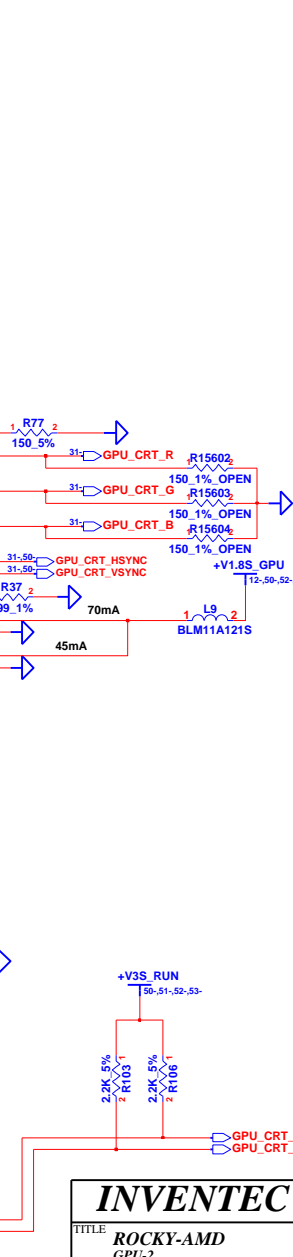
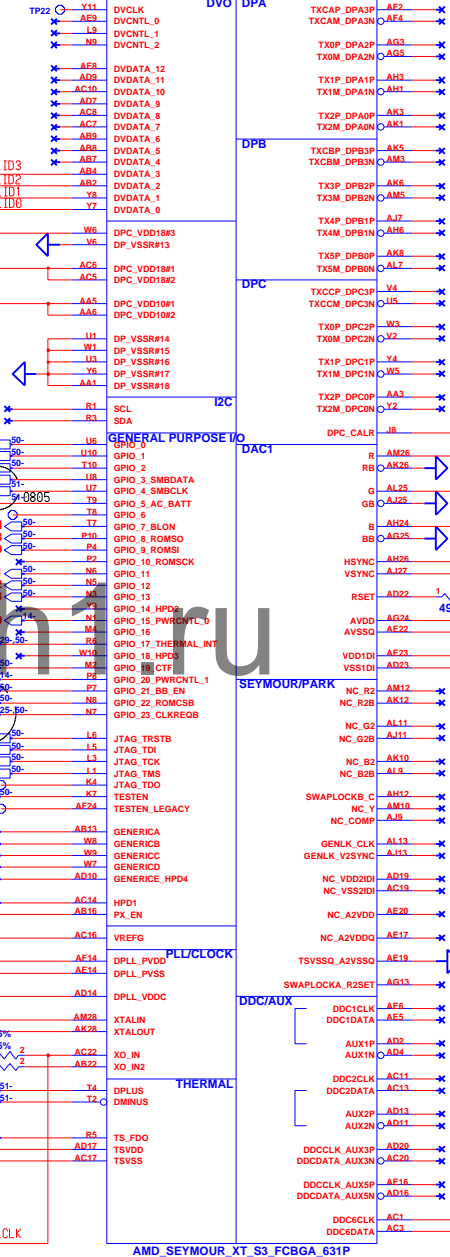
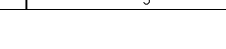
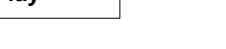
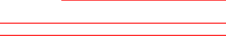
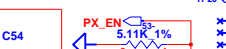
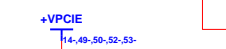
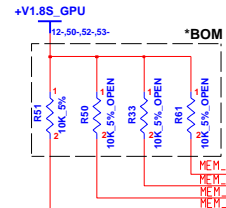
GPIO_13	GPIO_12	GPIO_11	Memory aperture size
0	0	1	512MB / 256MB (Default)
1	1	0	reserved



CET: GPU Critical temperature shang down 110C

POW_SW1	POW_SW0	+VDDC_GPU
0	0	1.1V
0	1	1V
1	0	0.95V
1	1	0.9V

Place TP344 out of GPU for calpella co-lay

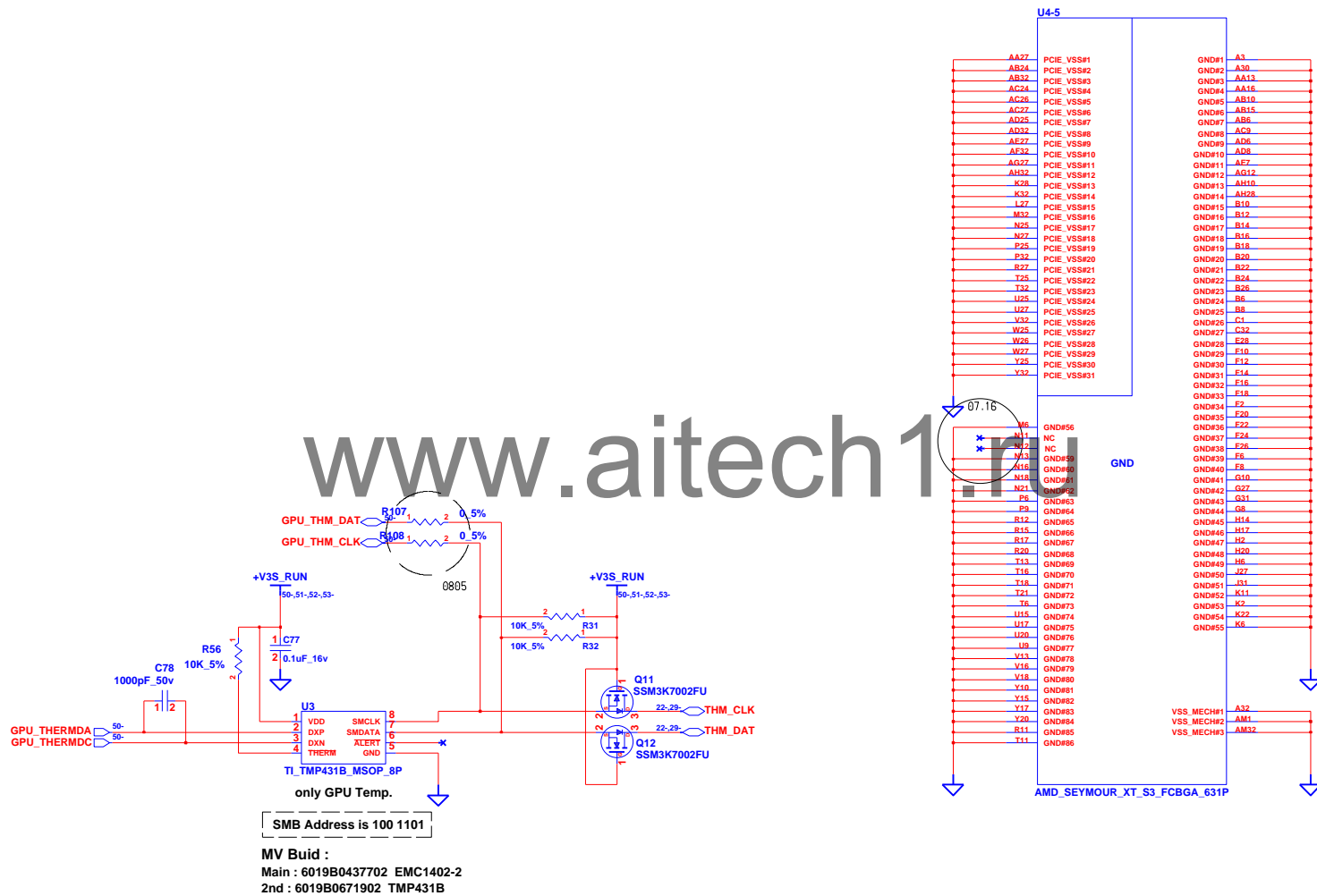


INVENTEC			
TITLE ROCKY-AMD GPU-2			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
SHEET		50	OF 60

CHANGE by Ken, Chiang

9-Jun-2010

8



INVENTEC

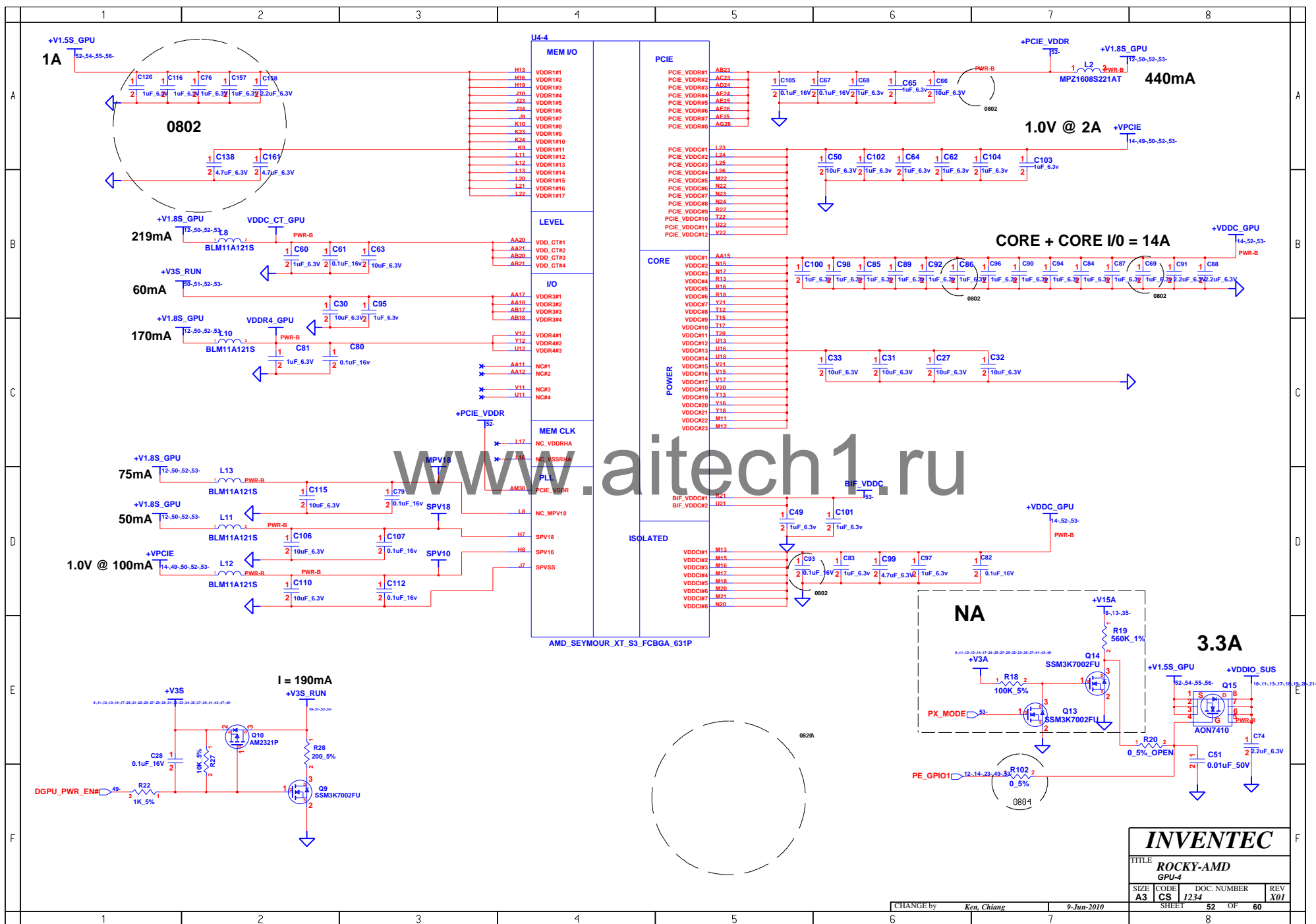
TITLE
ROCKY-AMD
GPU-3

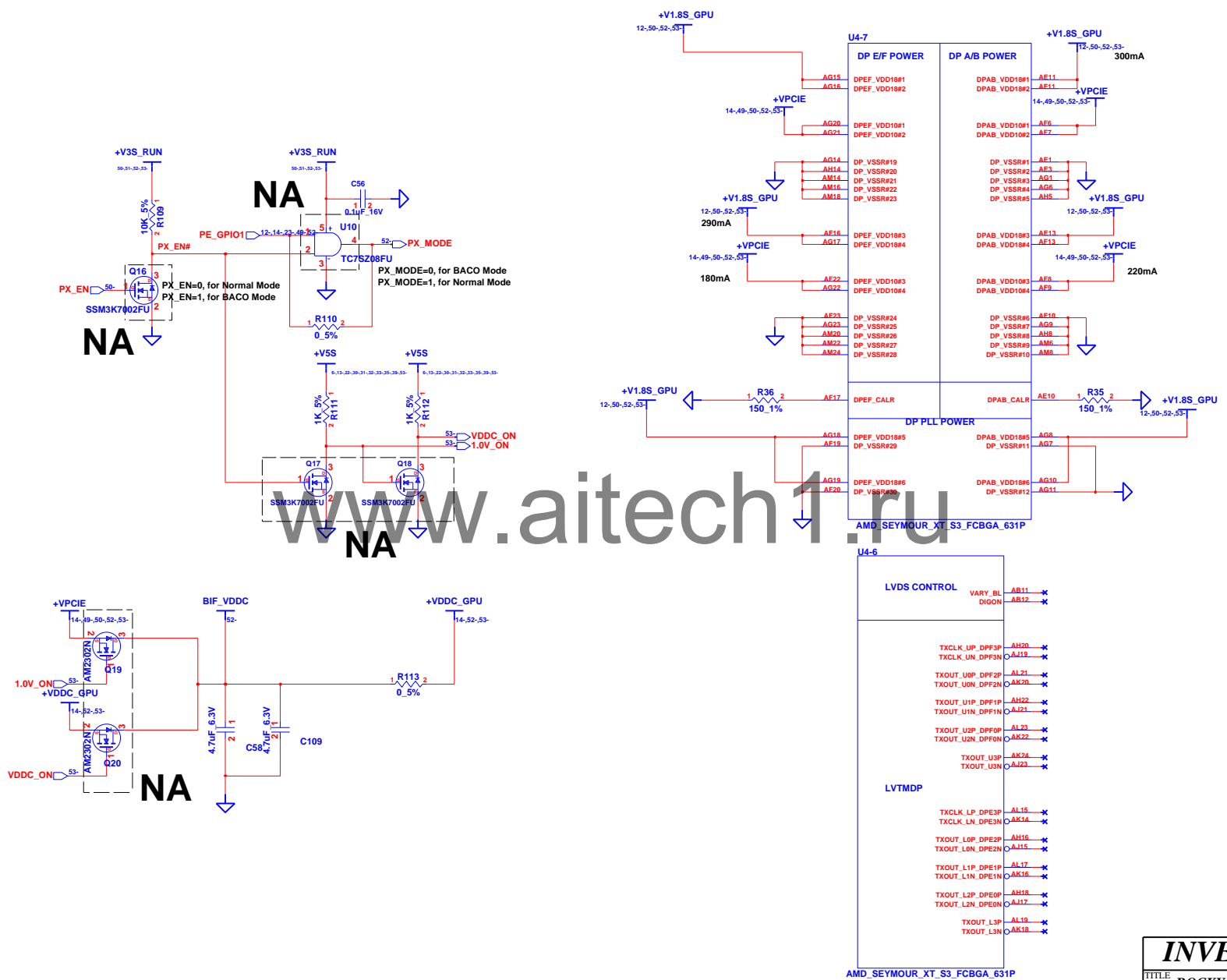
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1234	X01

CHANGE by Ken Chiang

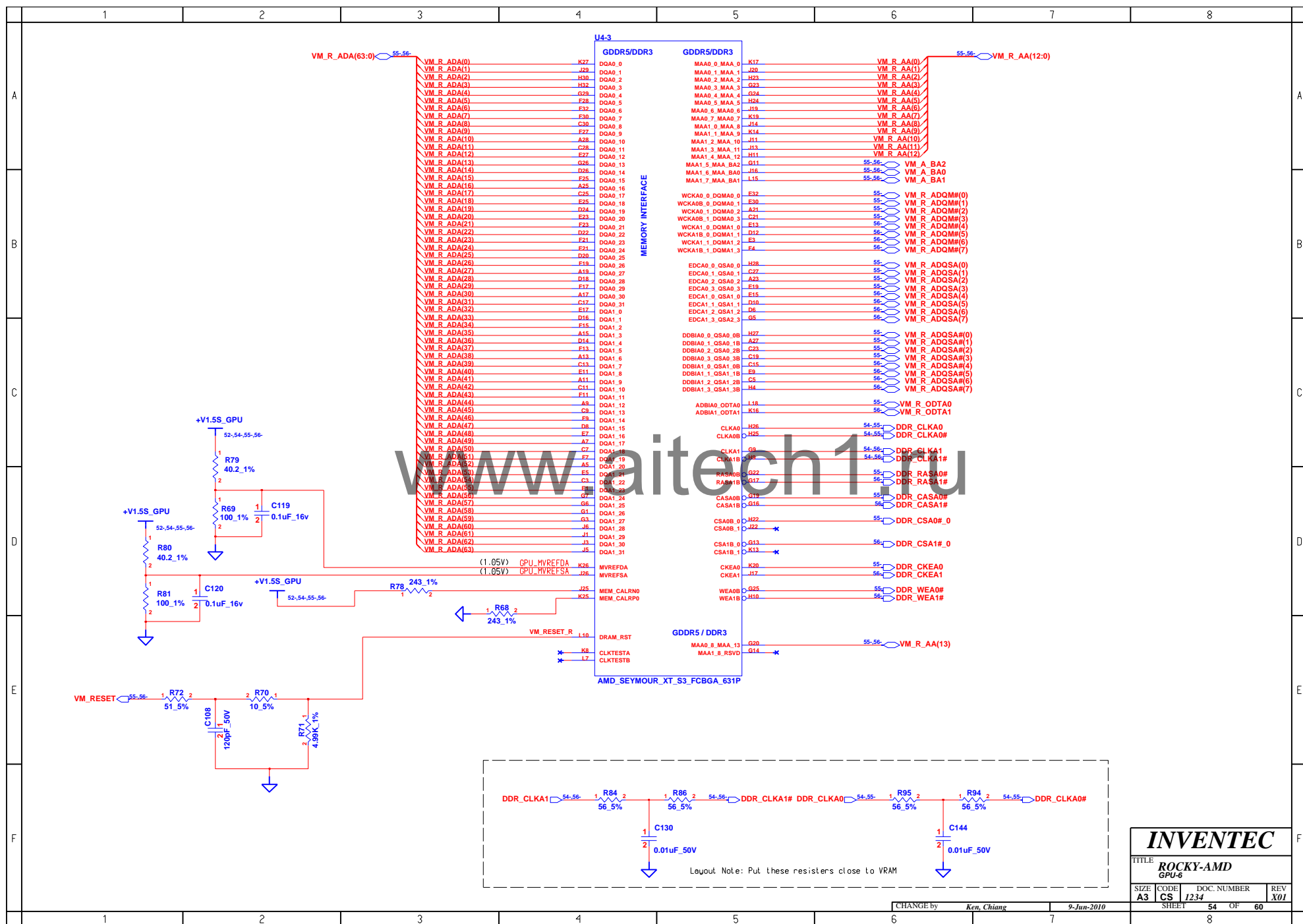
9-Jun-2010

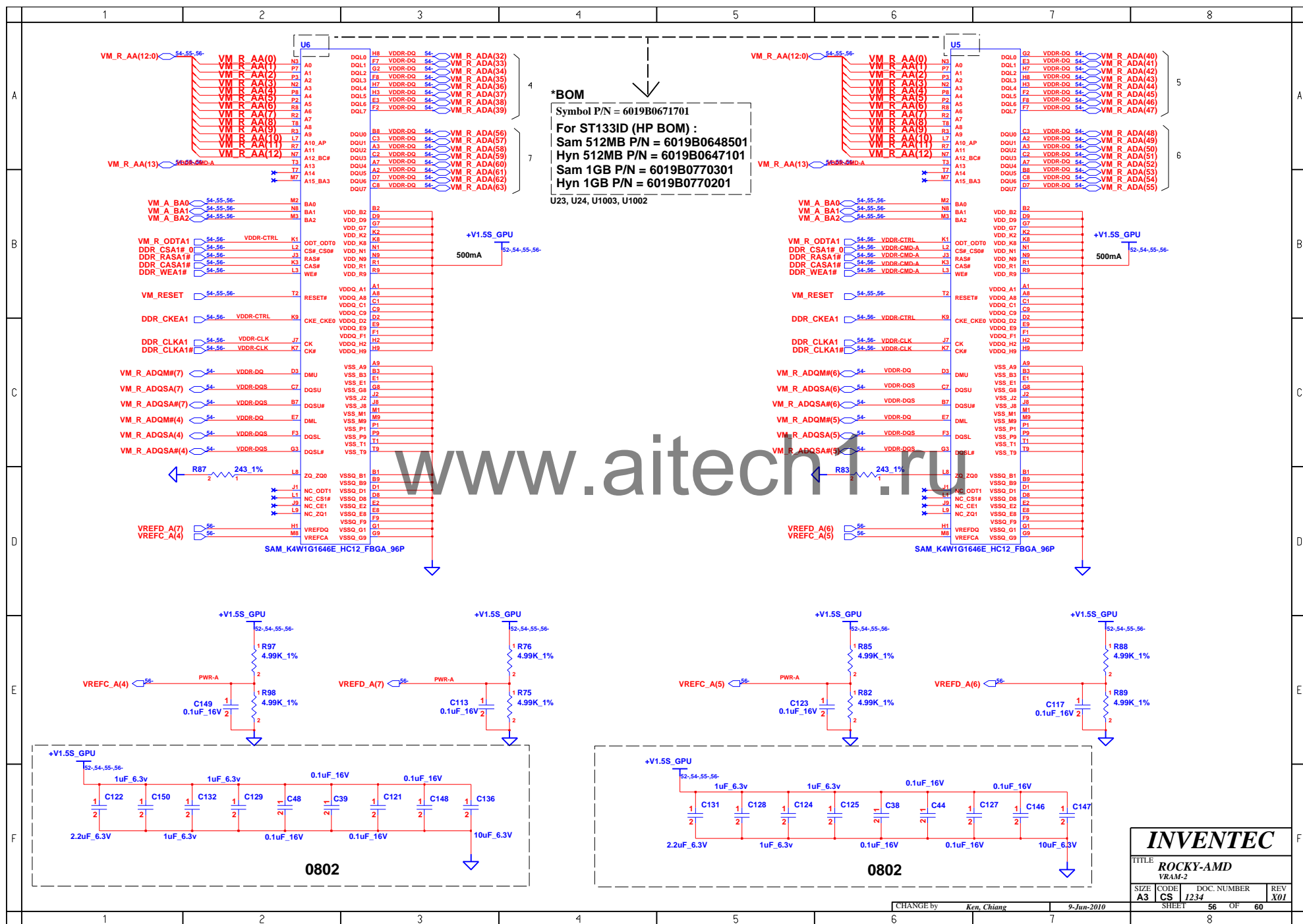
SHEET 51 OF 60





<i>INVENTEC</i>			
TITLE <i>ROCKY-AMD GPU-5</i>			
SIZE A3	CODE CS	DOC. NUMBER <i>1234</i>	REV <i>X01</i>
SHEET		53	OF 60





	1	2	3	4	5	6	7	8	
A									A
B									B
C									C
D									D
E									E
F									F
	1	2	3	4	5	6	7	8	

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INVENTEC			
TITLE ROCKY-AMD EXT USB CONN			
SIZE A3	CODE CS	DOC. NUMBER 1234	REV X01
CHANGE by Ken, Chiang		10-Aug-2010	
SHEET		57	OF 60

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A									A
B									B
C									C
D									D
E									E
F									F
						CHANGE by <i>Ken, Chiang</i>		10-Aug-2010	
						6	7	8	

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INVENTEC			
TITLE ROCKY-AMD			
SIZE A3	CODE CS	DOC. NUMBER <i>1234</i>	REV <i>X01</i>
SHEET		58	OF 60

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A									A
B									B
C									C
D									D
E									E
F									F
						CHANGE by <i>Ken, Chiang</i>		10-Aug-2010	
						6	7	8	

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INVENTEC			
TITLE ROCKY-AMD			
SIZE A3	CODE CS	DOC. NUMBER <i>1234</i>	REV <i>X01</i>
SHEET		59	OF 60

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A									A
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C									C
D									D
E									E
F									F
						CHANGE by <i>Ken, Chiang</i>		10-Aug-2010	
						6	7	8	

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INVENTEC			
TITLE ROCKY-AMD			
SIZE A3	CODE CS	DOC. NUMBER <i>1234</i>	REV <i>X01</i>
SHEET		60	OF 60